LMF Laboratoire Méthodes Formelles

université PARIS-SACLAY

Introduction à la compilation

Polytech'Paris-Saclay– 4ème année –

Generation du Code

Burkhart Wolff

Plan of this Course

Plan of this Course

Plan of this Course

- A Bluffers Guide to Computer Architectures

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- A Bluffers Guide to Computer Architectures
- Assembler and Machine Code

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- Optimizations

(Standard)
Computer Architectures

Background: Computer Architecture

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- Basics: vonNeumann Architecture

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    - Modern Architectures

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von Neumann Architecture

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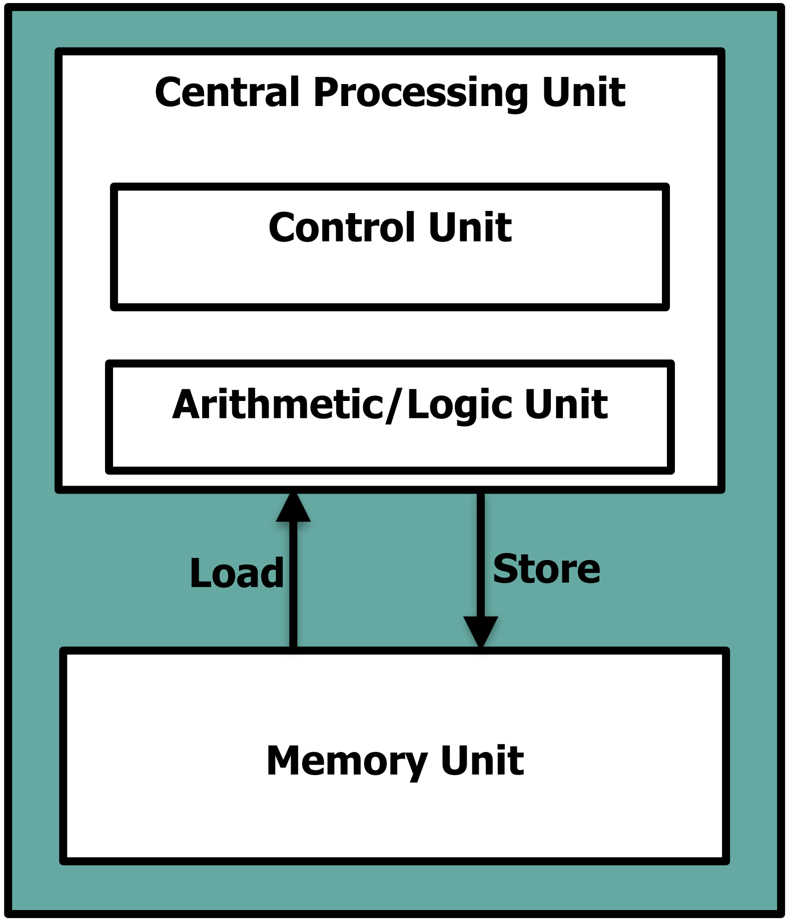

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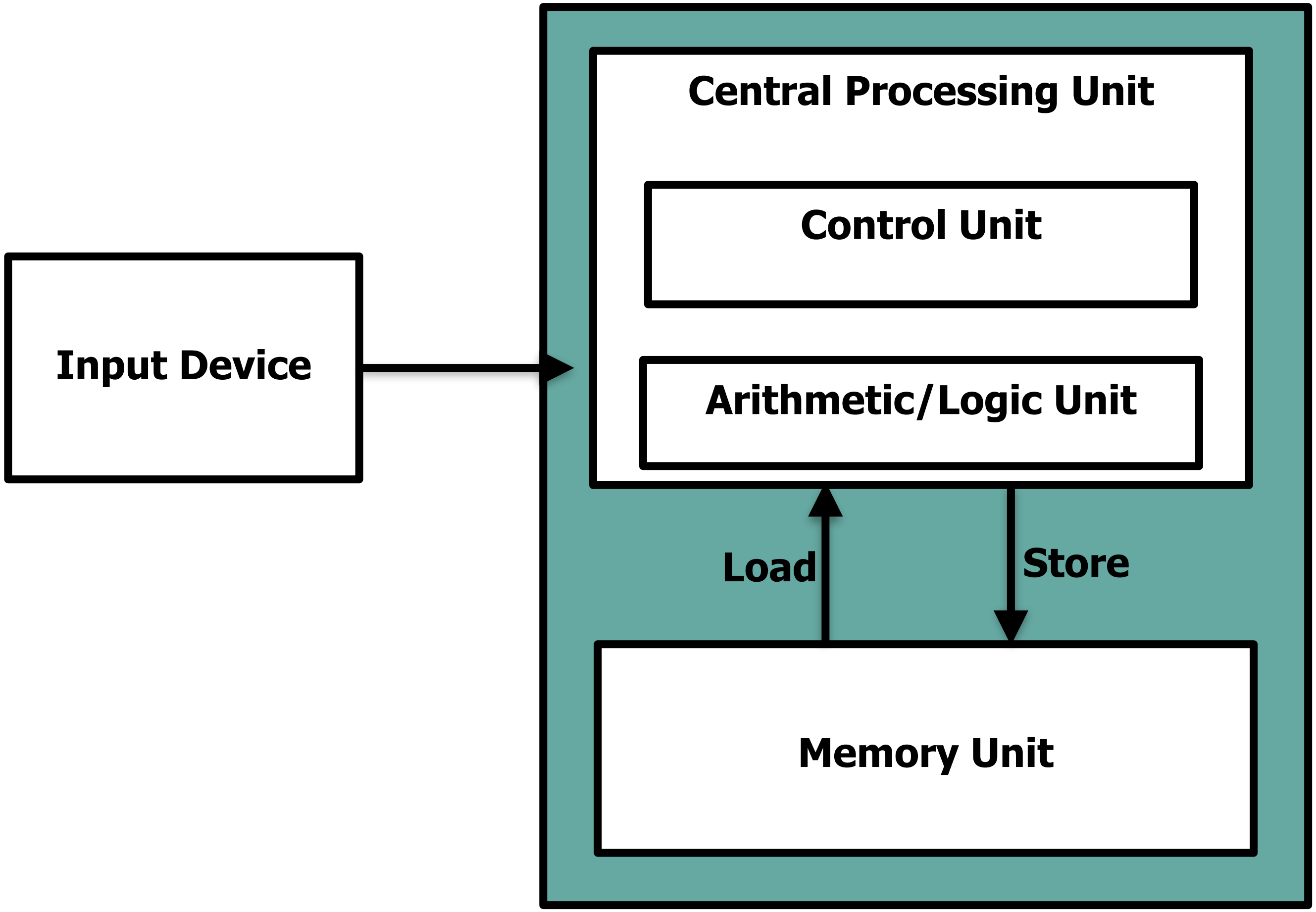

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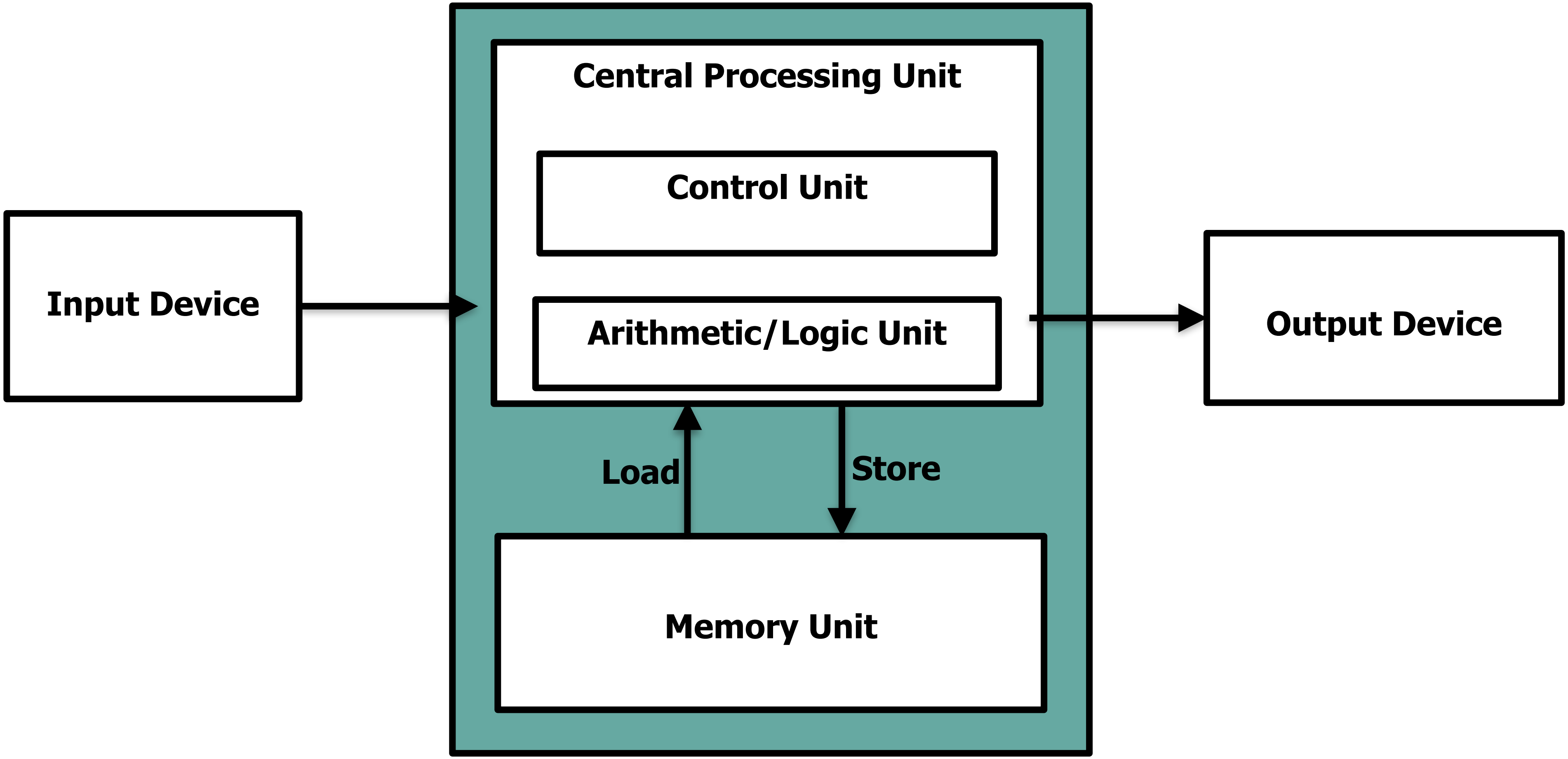

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von Neumann Architecture

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  - CPU, ALU,
  - words & adresses,
    for data and programs
  - slow memory, fast registers,
    i.e. load and store ops
  - 2s-complements for numbers,

von Neumann Architecture

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- A more recent architecture model:

von Neumann Architecture

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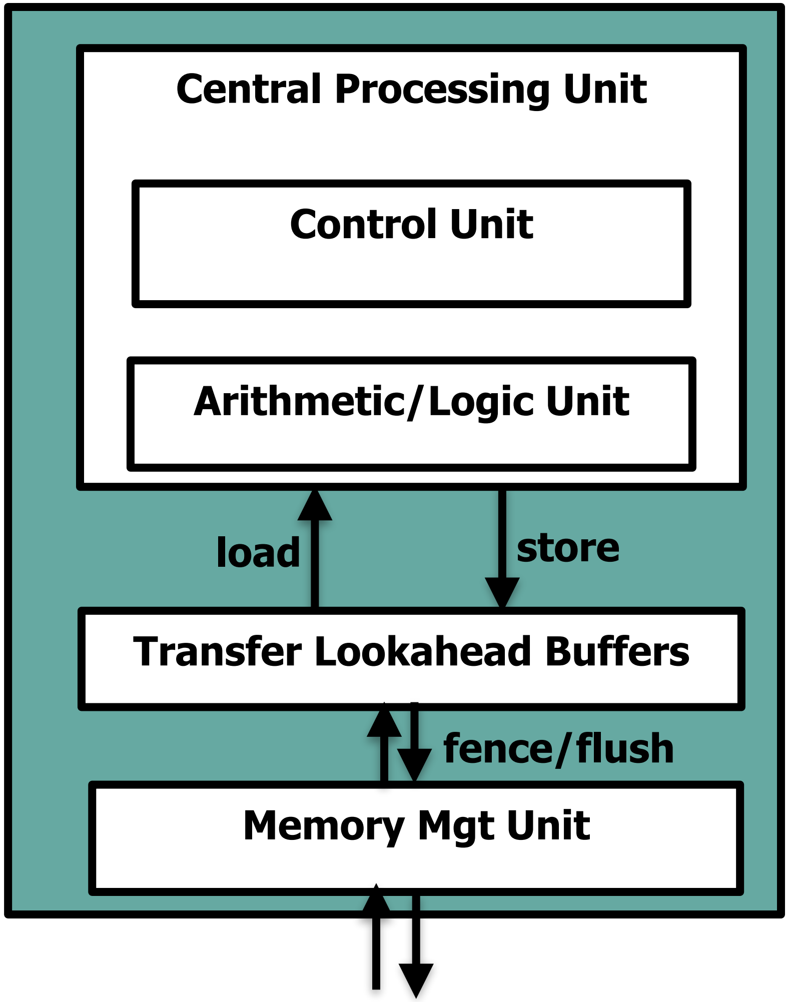

von Neumann Architecture

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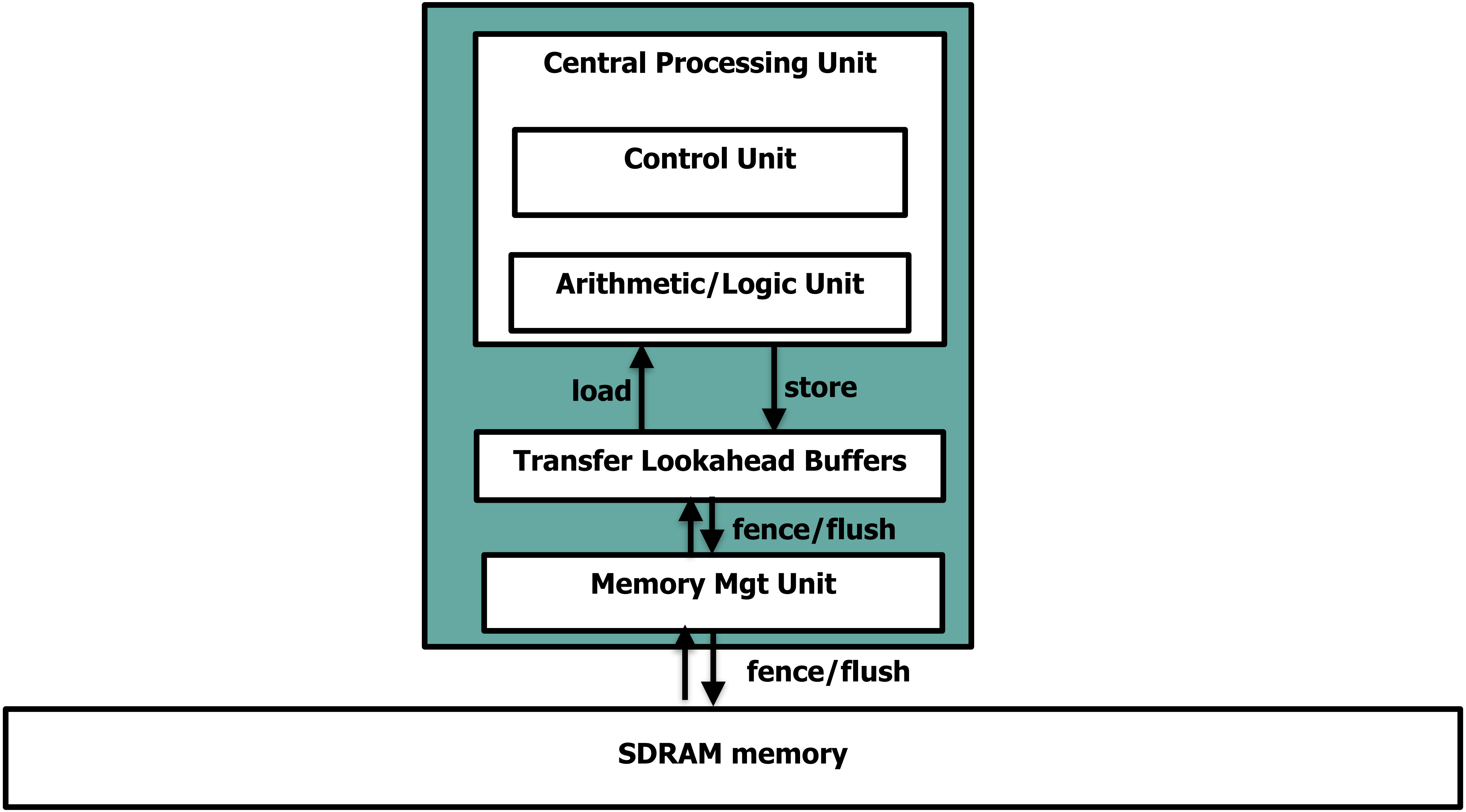

Central Processing Unit

Control Unit

Arithmetic/Logic Unit

load

store

Transfer Lookahead Buffers

fence/flush

Memory Mgt Unit

fence/flush

SDRAM memory

von Neumann Architecture

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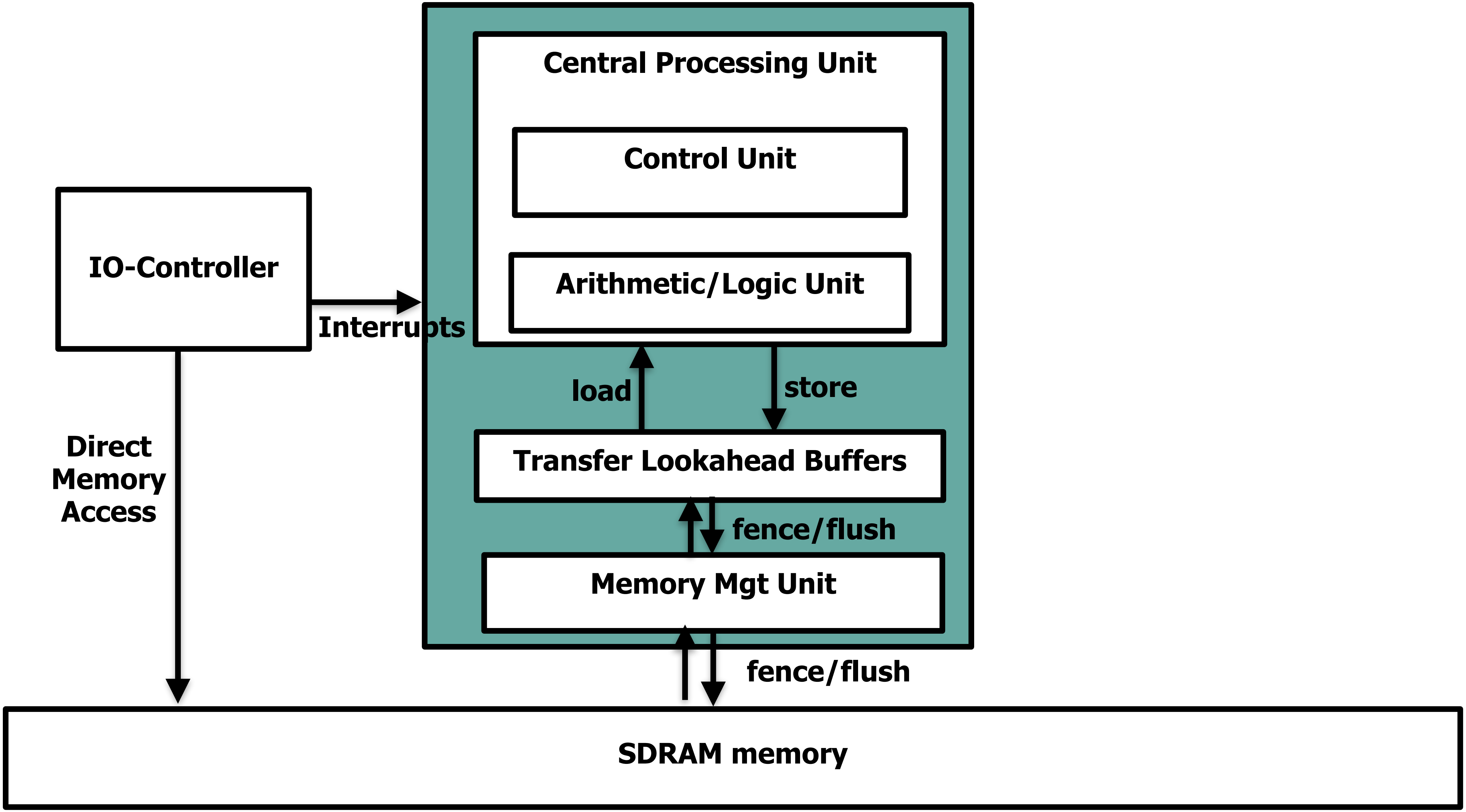

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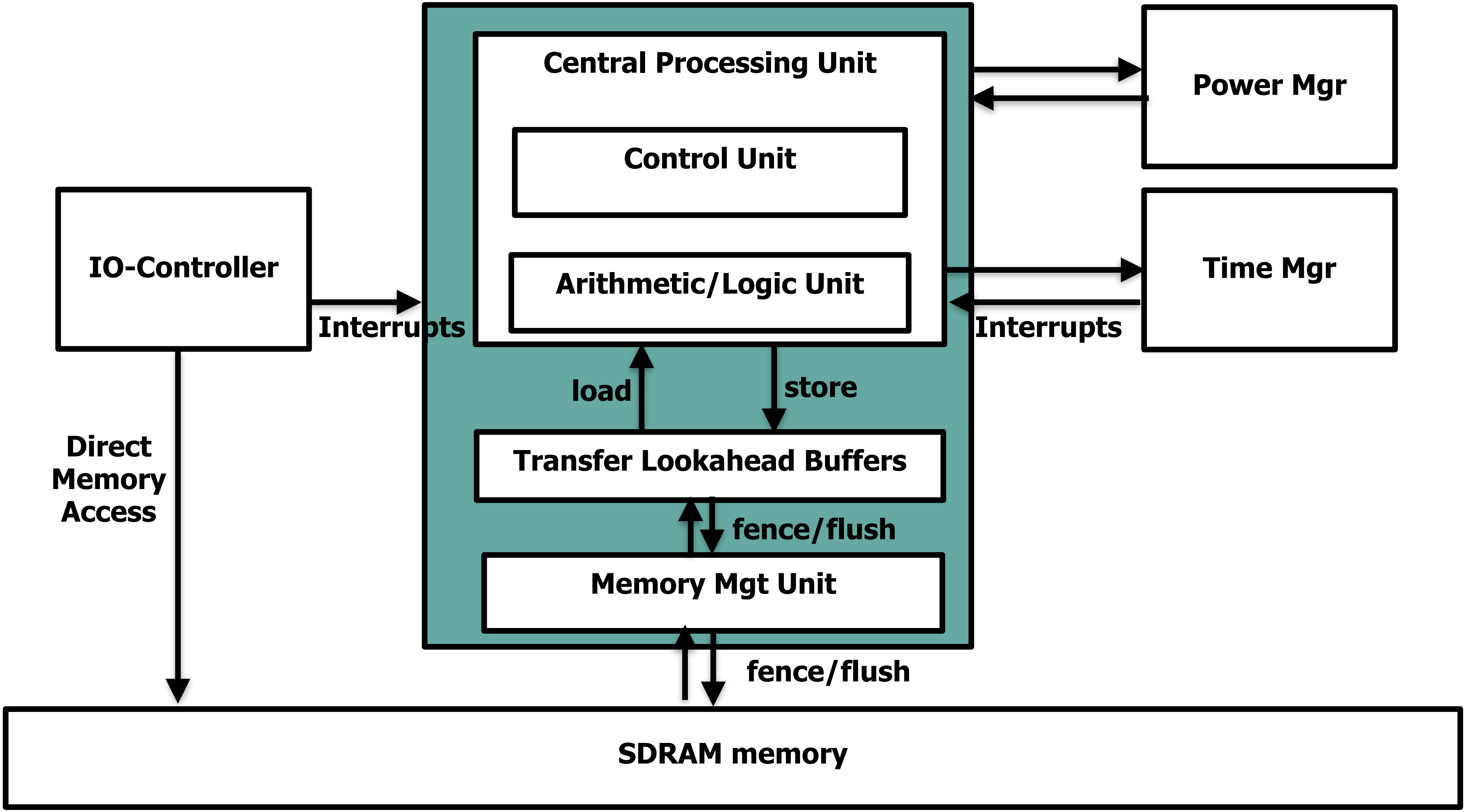

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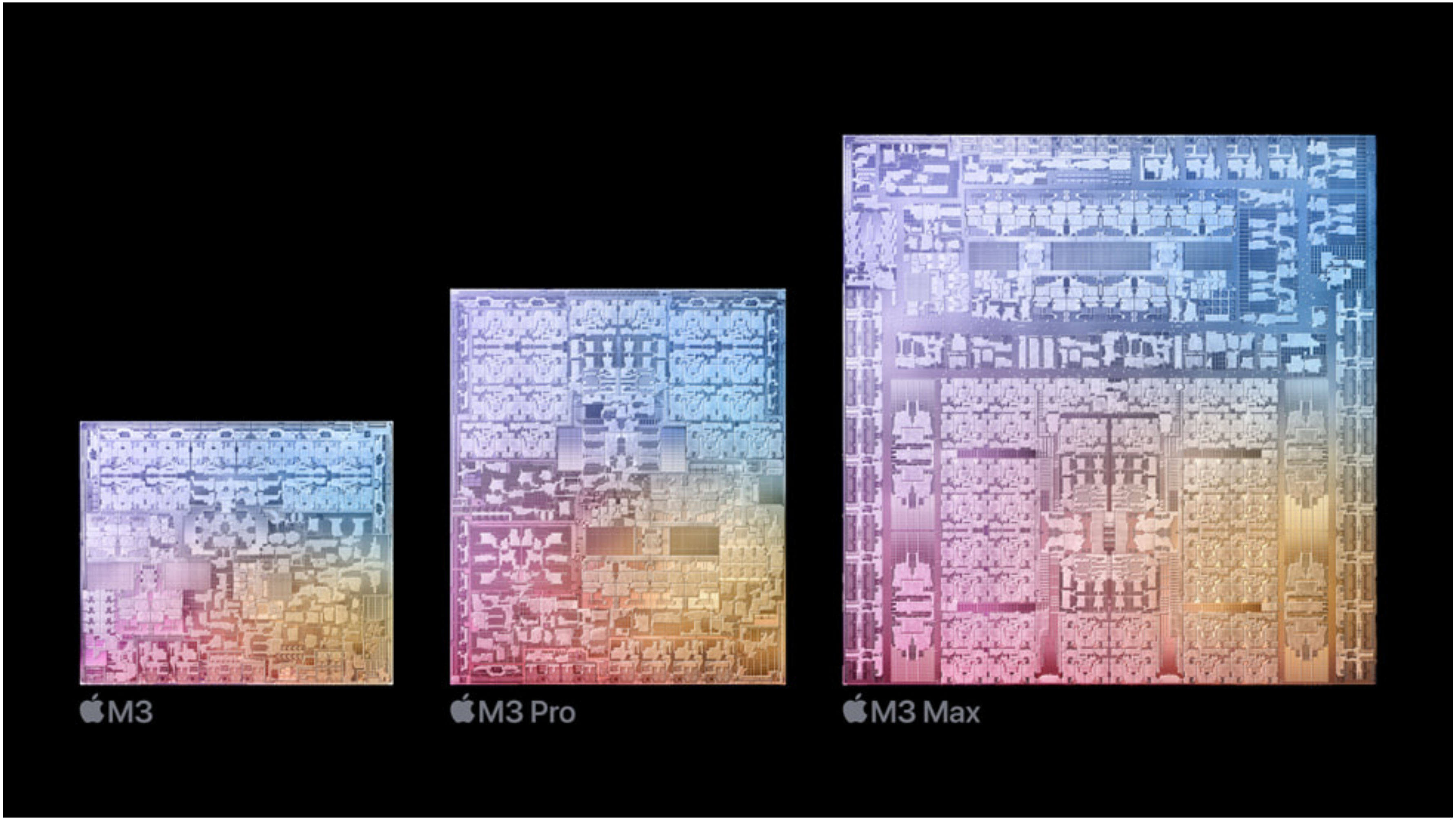


von Neumann Architecture

- Current ARM variants (MX, © Apple):
  - multi-cores basically the same
  - but graphical processing units,
  - … neural engines,
  - … and lots of stuff.

Compilation to Assembly Languages (Reminder)

Source Code to Assembly Code

Source code fib.c

```
int64_t fib(int64_t n) {
  if (n < 2) return n;
  return (fib(n-1) + fib(n-2));
}
```

```
$ clang -O3 fib.c -S
```

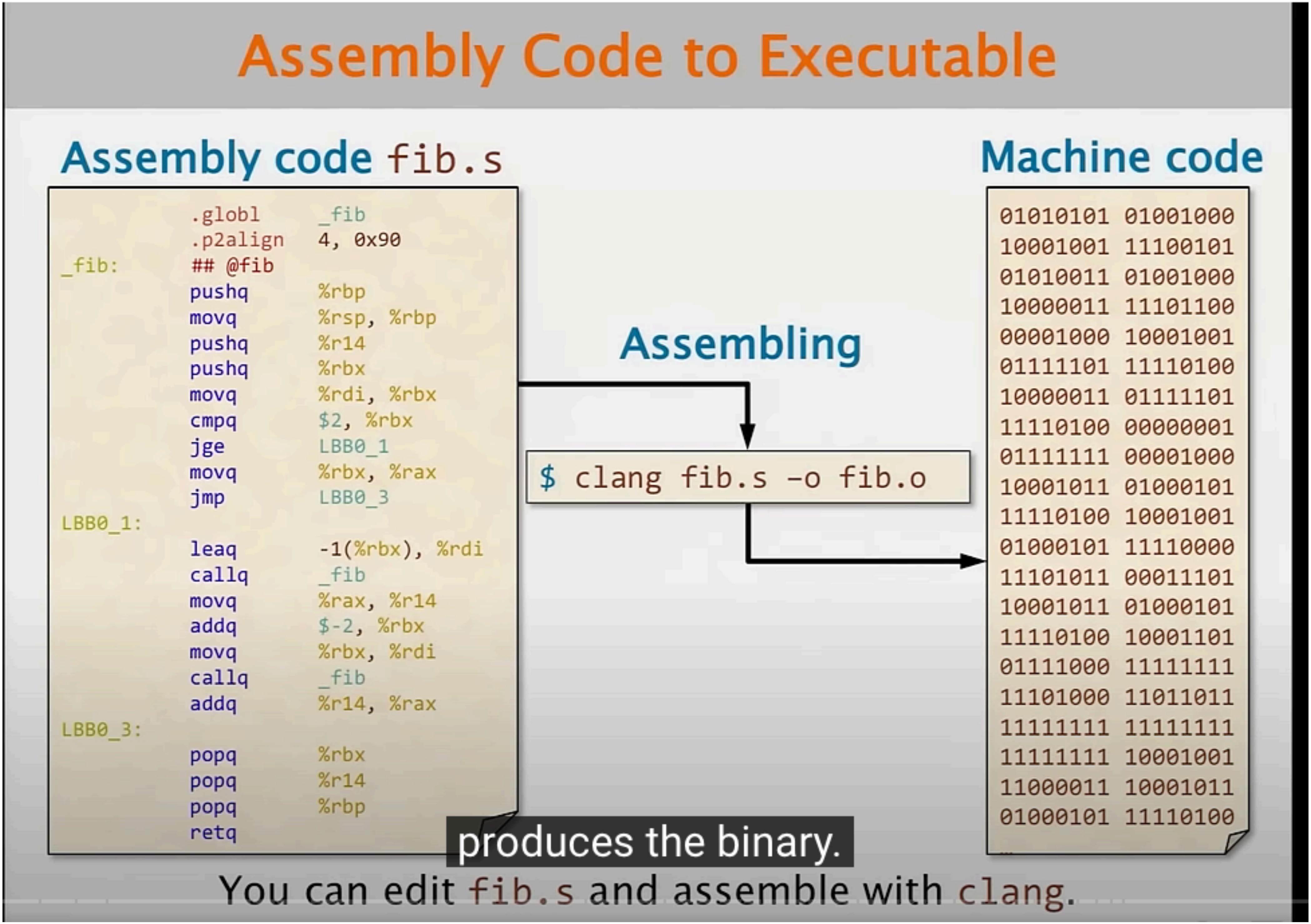
Assembly language provides a convenient symbolic representation of machine code.

Assembly code fib.s

```
            .globl      _fib
            .p2align    4, 0x90
_fib:       ## @fib
            pushq       %rbp
            movq        %rsp, %rbp
            pushq       %r14
            pushq       %rbx
            movq        %rdi, %rbx
            cmpq        $2, %rbx
            jge         LBB0_1
            movq        %rbx, %rax
            jmp         LBB0_3
LBB0_1:
            leaq        -1(%rbx), %rdi
            callq       _fib
            movq        %rax, %r14
            addq        $-2, %rbx
            movq        %rbx, %rdi
            callq       _fib
            addq        %r14, %rax
LBB0_3:
            popq        %rbx
            popq        %r14
            popq        %rbp
            retq
```

See http://sourceware.org/binutils/docs/as/index.html.

The next stage is the source code to assembly code.



Assembly Code to Executable

Assembly code fib.s

```
            .globl      _fib
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_fib:       ## @fib
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            addq        %r14, %rax
LBB0_3:
            popq        %rbx
            popq        %r14
            popq        %rbp
            retq
```

Assembling

```
$ clang fib.s -o fib.o
```

Machine code

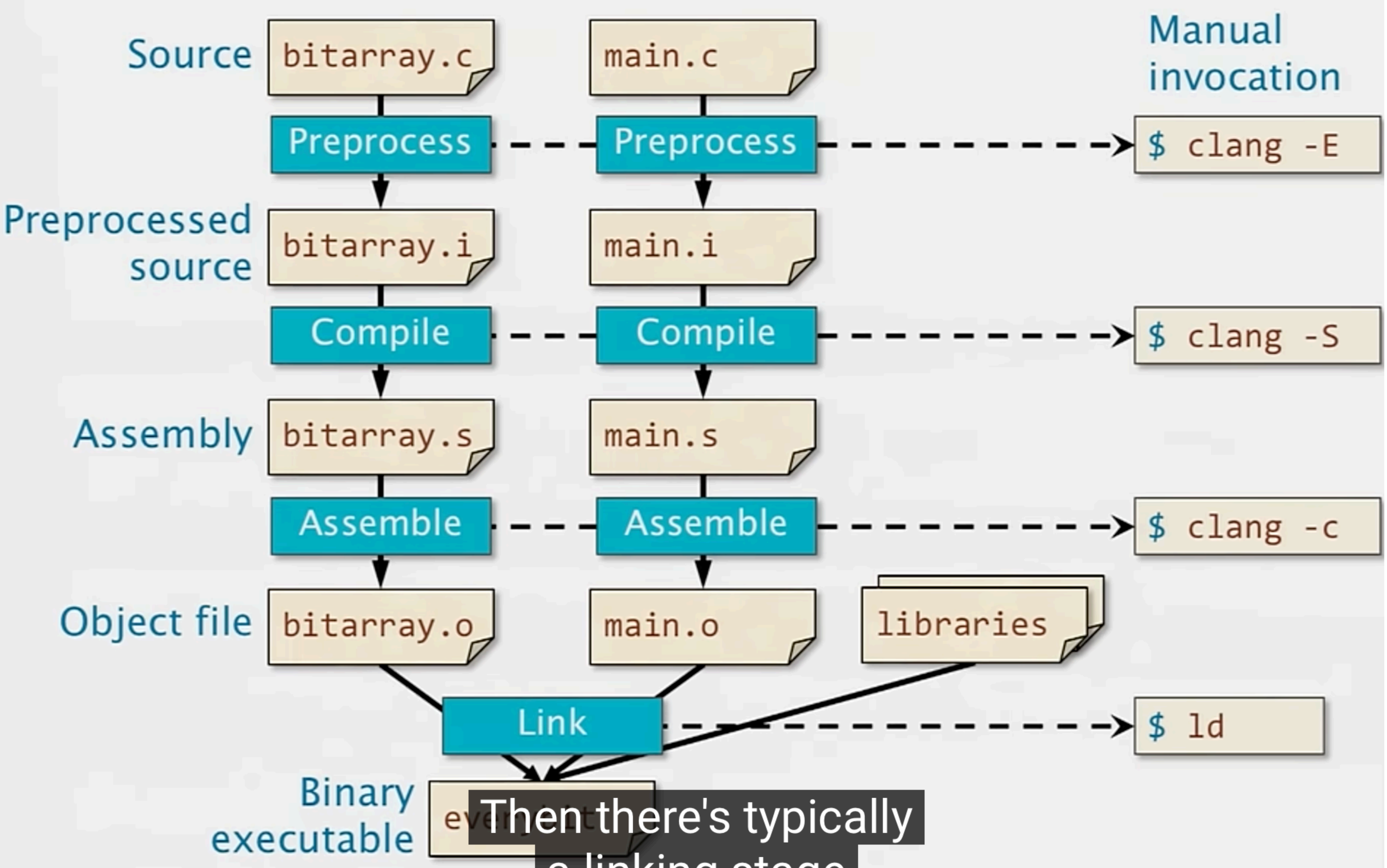
```
01010101 01001000
10001001 11100101
01010011 01001000
10000011 11101100
00001000 10001001
01111101 11110100
10000011 01111101
11110100 00000001
01111111 00001000
10001011 01000101
11110100 10001001
01000101 11110000
11101011 00011101
10001011 01000101
11110100 10001101
01111000 11111111
11101000 11011011
11111111 11111111
11111111 10001001
11000011 10001011
01000101 11110100
...
```

produces the binary.

You can edit fib.s and assemble with clang.

En réalité c'est encore trop simple … (clang LLVM)

The Four Stages of Compilation

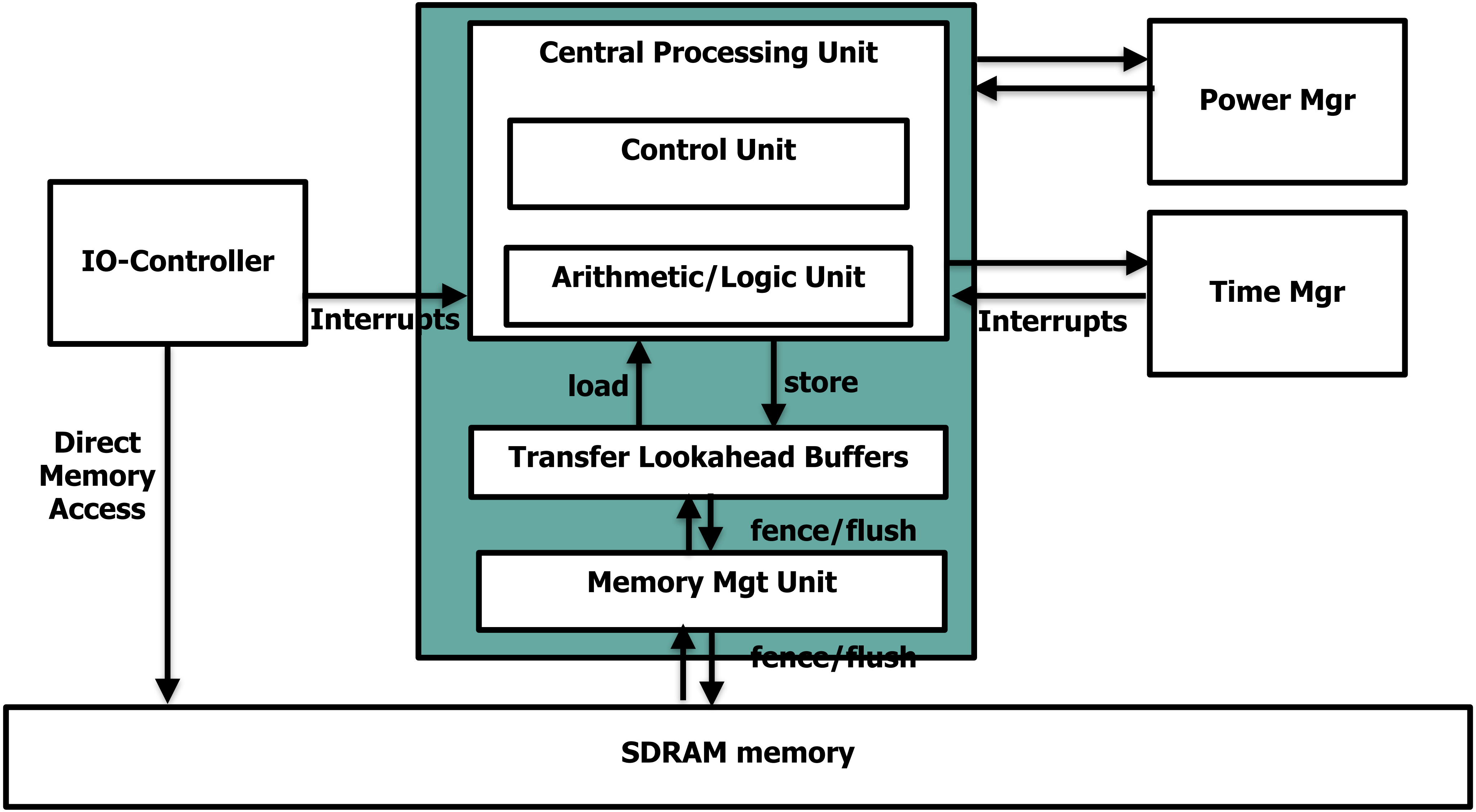


Then there's typically a linking stage

The Core:
Instruction Set Architectures
(ISA)

The Core of the Architecture

- Fortunately, a lot is largely irrelevant (except for embedded system developers)



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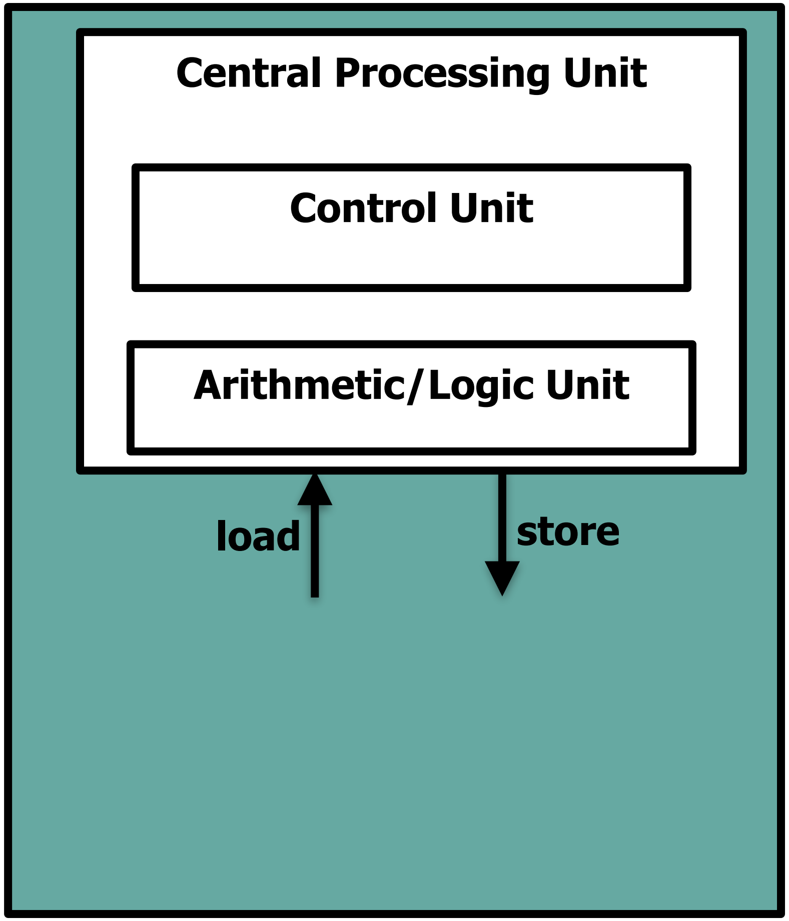

The Core : Computer Architecture

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The Core : Computer Architecture

- Instruction Sets Architectures (ISA ’ s) are reflected directly in assembly languages
- There are typically different processors “implementing” a particular ISA (- family)
- Nowadays, we see 3 major ISA families:
  - X86 (Intel and AMD processors)
  - ARM (lots of vendors, e.g. Apple)
  - RISC-V (open source, getting traction ...)
- ... plus virtual machine ISA’s like LLVM or JVM

An Example ISA: ARM Cortex M

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- What constitutes an ISA ?

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- What constitutes an ISA ?
  - where the processor stores or obtains information

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- What constitutes an ISA ?
  - where the processor stores or obtains information
    - registers

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- What constitutes an ISA ?
    - where the processor stores or obtains information
        - registers
        - memory

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  - how the processor manipulates data

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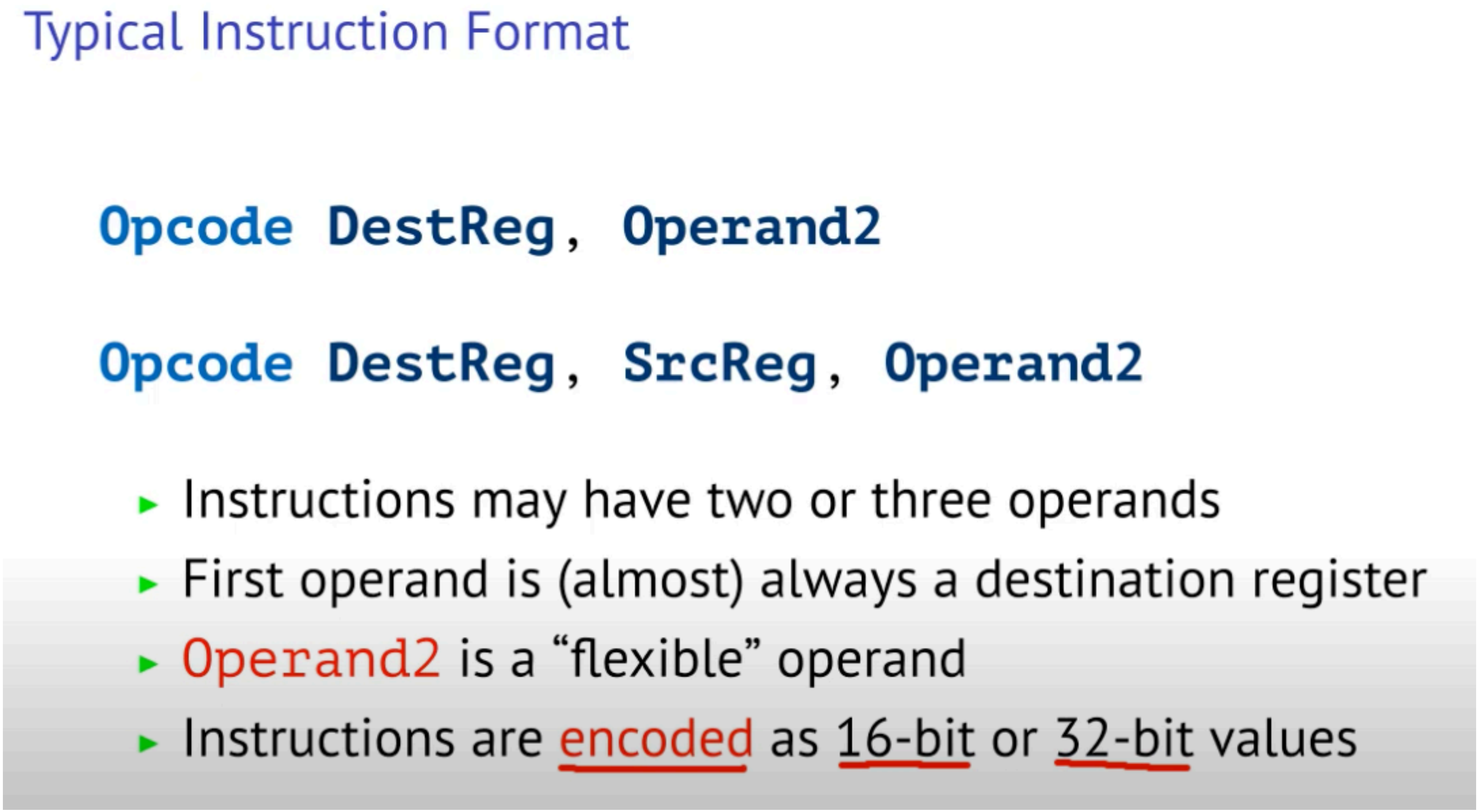

Typical Instruction Format

```
Opcode DestReg, Operand2

Opcode DestReg, SrcReg, Operand2
```

- Instructions may have two or three operands
- First operand is (almost) always a destination register
- Operand2 is a “flexible” operand
- Instructions are encoded as 16-bit or 32-bit values

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- Sources:

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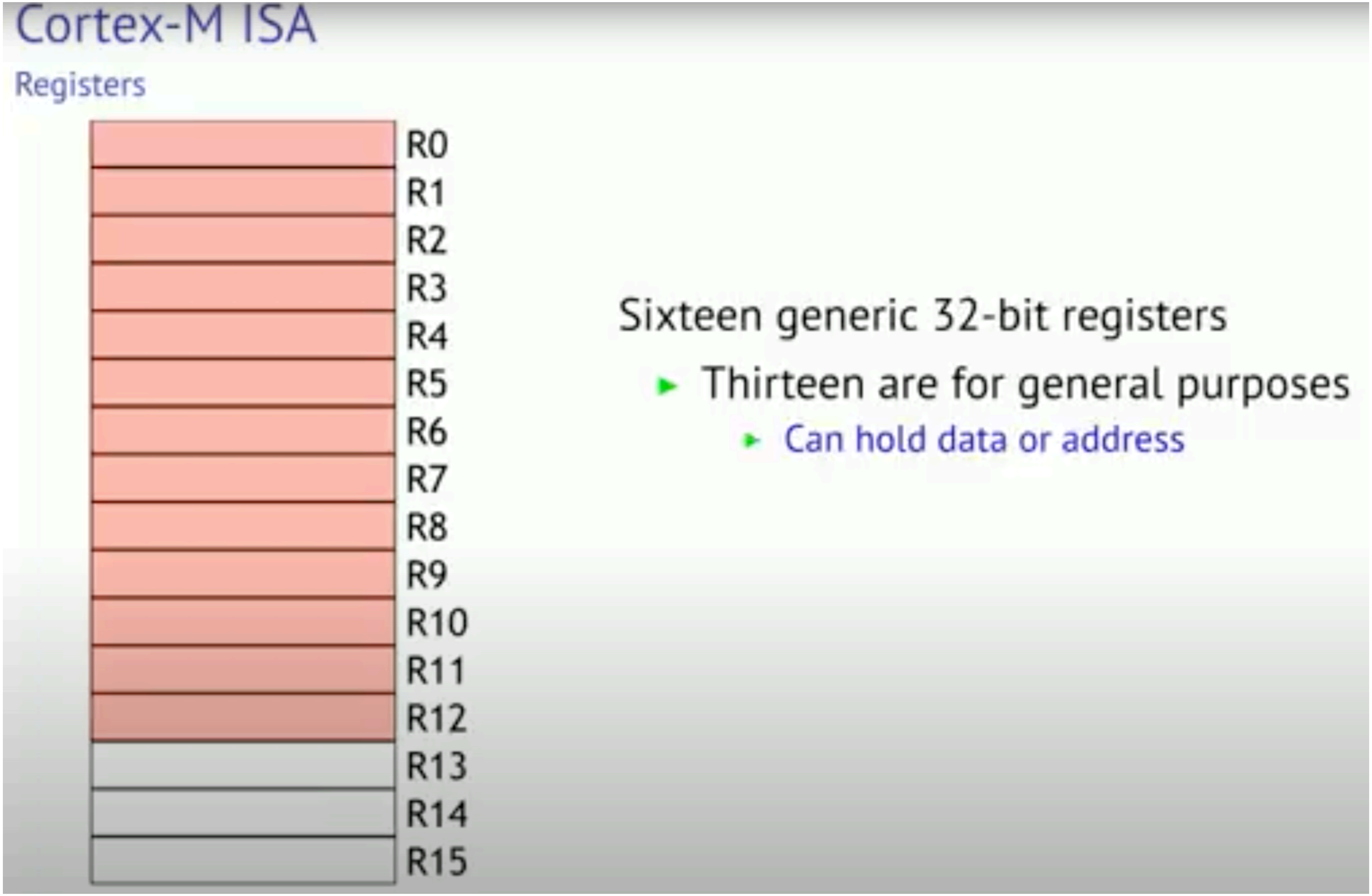

Cortex-M ISA

Registers

R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15

Sixteen generic 32-bit registers

- Thirteen are for general purposes
  - Can hold data or address

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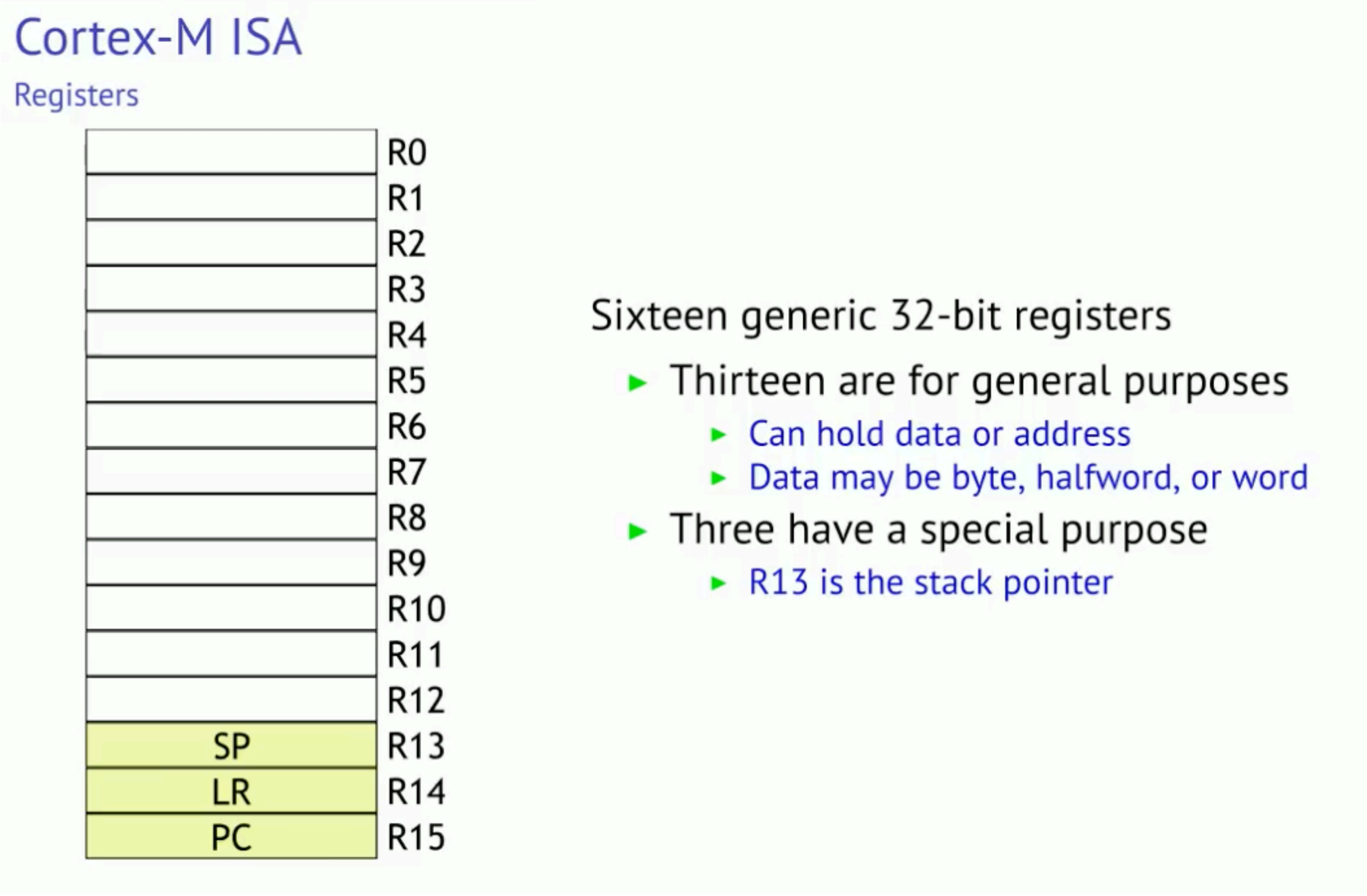

Cortex-M ISA

Registers

	R0
	R1
	R2
	R3
	R4
	R5
	R6
	R7
	R8
	R9
	R10
	R11
	R12
SP	R13
LR	R14
PC	R15

Sixteen generic 32-bit registers

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  - Can hold data or address
  - Data may be byte, halfword, or word
- Three have a special purpose
  - R13 is the stack pointer

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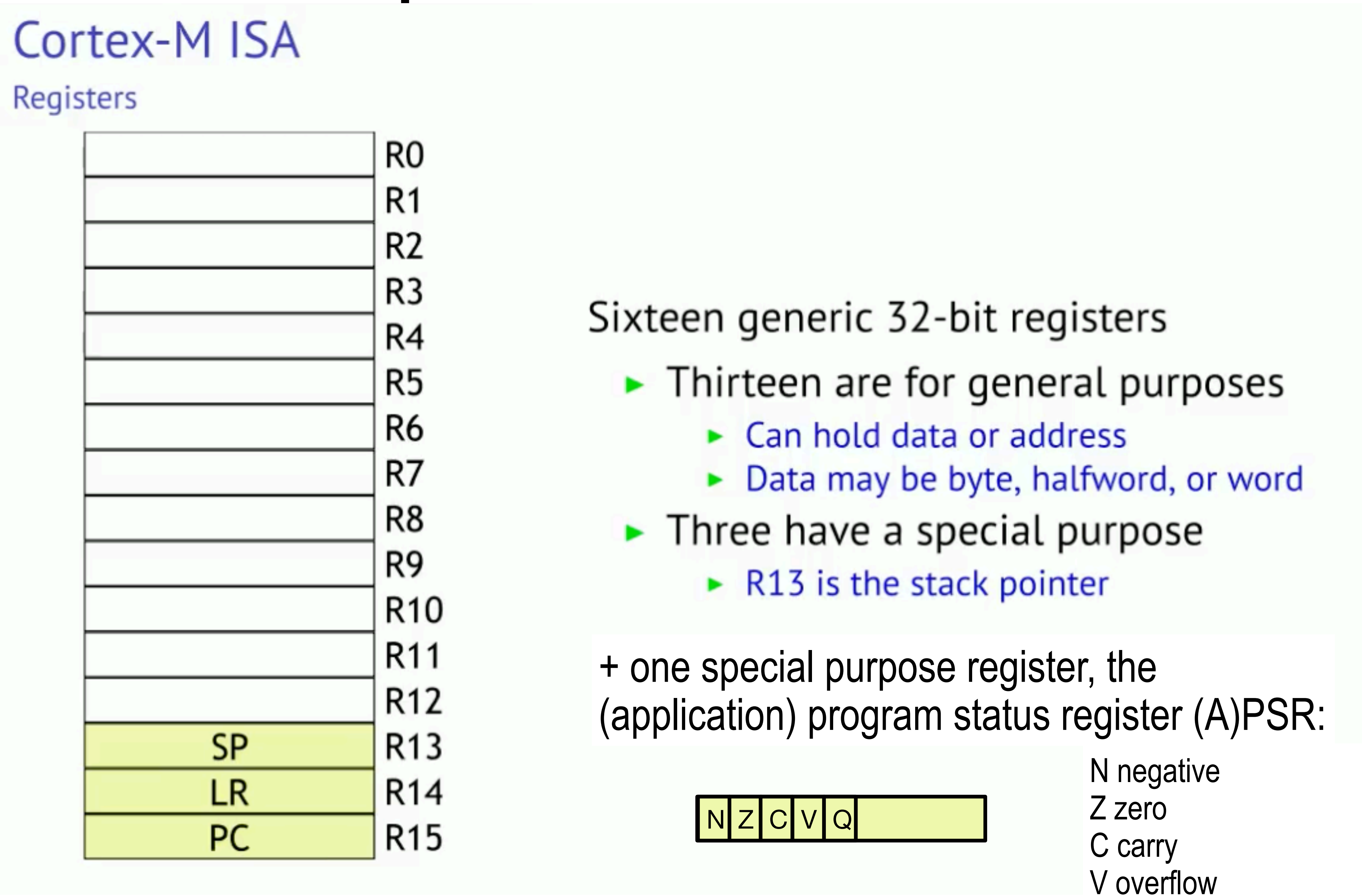

Cortex-M ISA

Registers

Sixteen generic 32-bit registers

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  - Can hold data or address
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+ one special purpose register, the (application) program status register (A)PSR:

N negative
Z zero
C carry
V overflow
Q saturation

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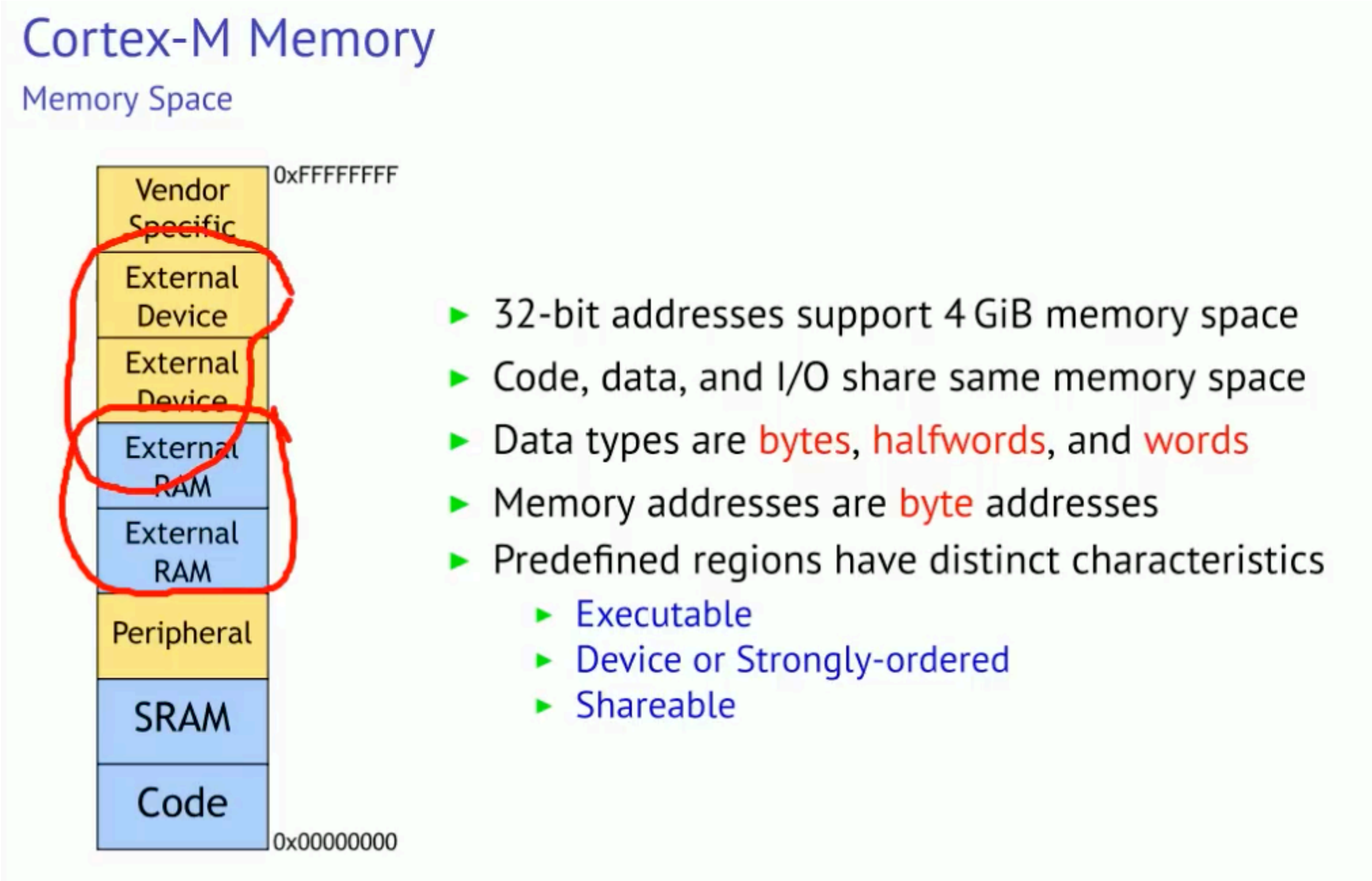

Cortex-M Memory

Memory Space

- 32-bit addresses support 4 GiB memory space
- Code, data, and I/O share same memory space
- Data types are bytes, halfwords, and words
- Memory addresses are byte addresses
- Predefined regions have distinct characteristics
  - Executable
  - Device or Strongly-ordered
  - Shareable

An Example ISA: ARM Cortex 7

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- Register Transfer Operations

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- Register Transfer Operations

0x00000011	R0
0x00000A00	R1
0xFFFFFFFB	R2
0xFEEDC0DE	R3
0x00000A00	R4
	R5
	R6
	R7
	R8
	R9
	R10
	R11
	R12
	R13
	R14

```
MOV   R0, #0x11
MOV   R1, #2560
MVN   R2, #4
MOVW  R3, #0xC0DE
MOVT  R3, #0xFEED
MOV   R4, R1
```

An Example ISA: ARM Cortex 7

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- Basic Load/Store operations

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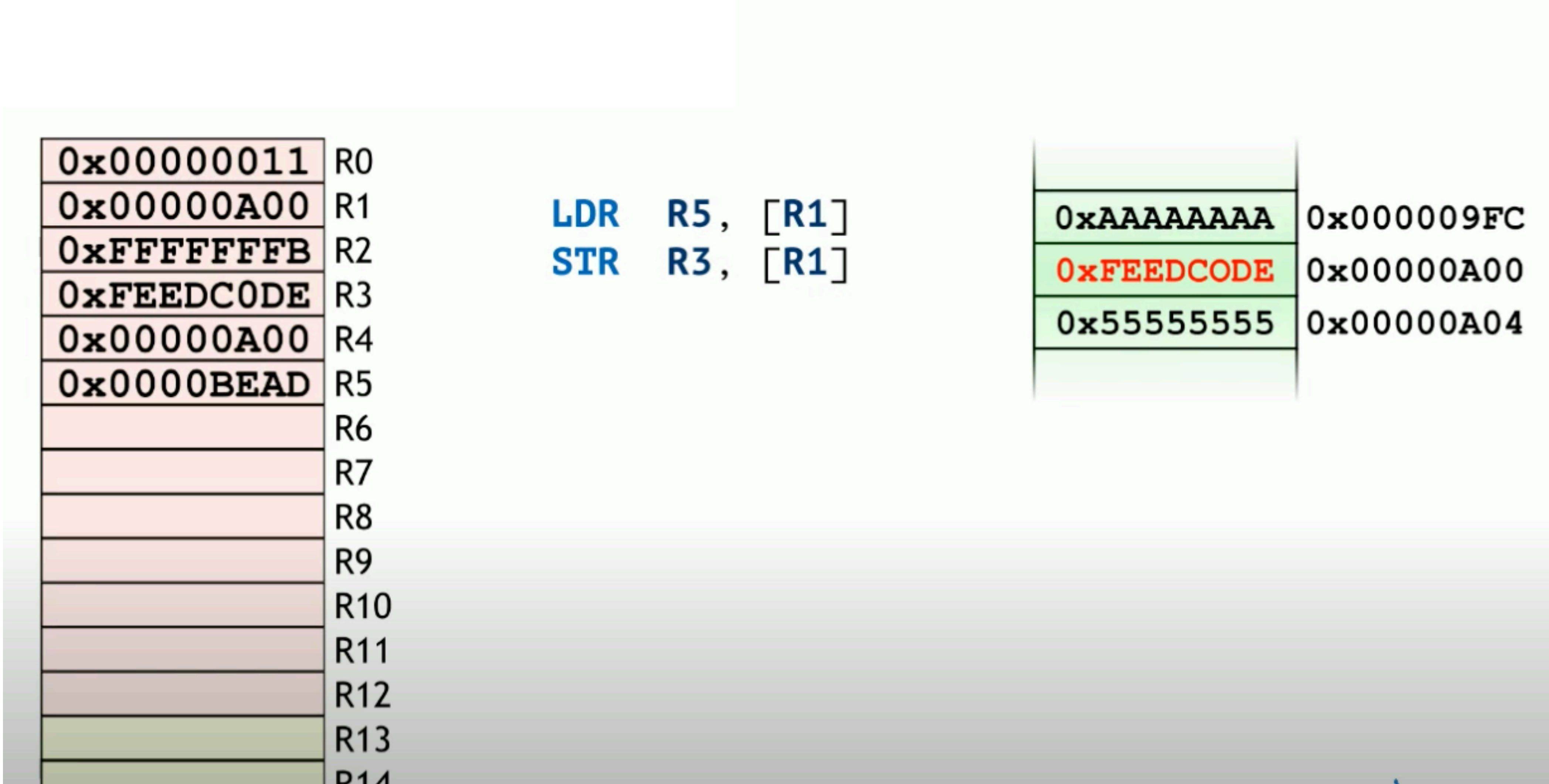

0x00000011	R0
0x00000A00	R1
0xFFFFFFFB	R2
0xFEEDC0DE	R3
0x00000A00	R4
0x0000BEAD	R5
	R6
	R7
	R8
	R9
	R10
	R11
	R12
	R13
	R14

```
LDR   R5, [R1]
STR   R3, [R1]
```

0xAAAAAAAA	0x000009FC
0xFEEDC0DE	0x00000A00
0x55555555	0x00000A04

An Example ISA: ARM Cortex 7

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- Basic Load/Store with offsets (for arrays)

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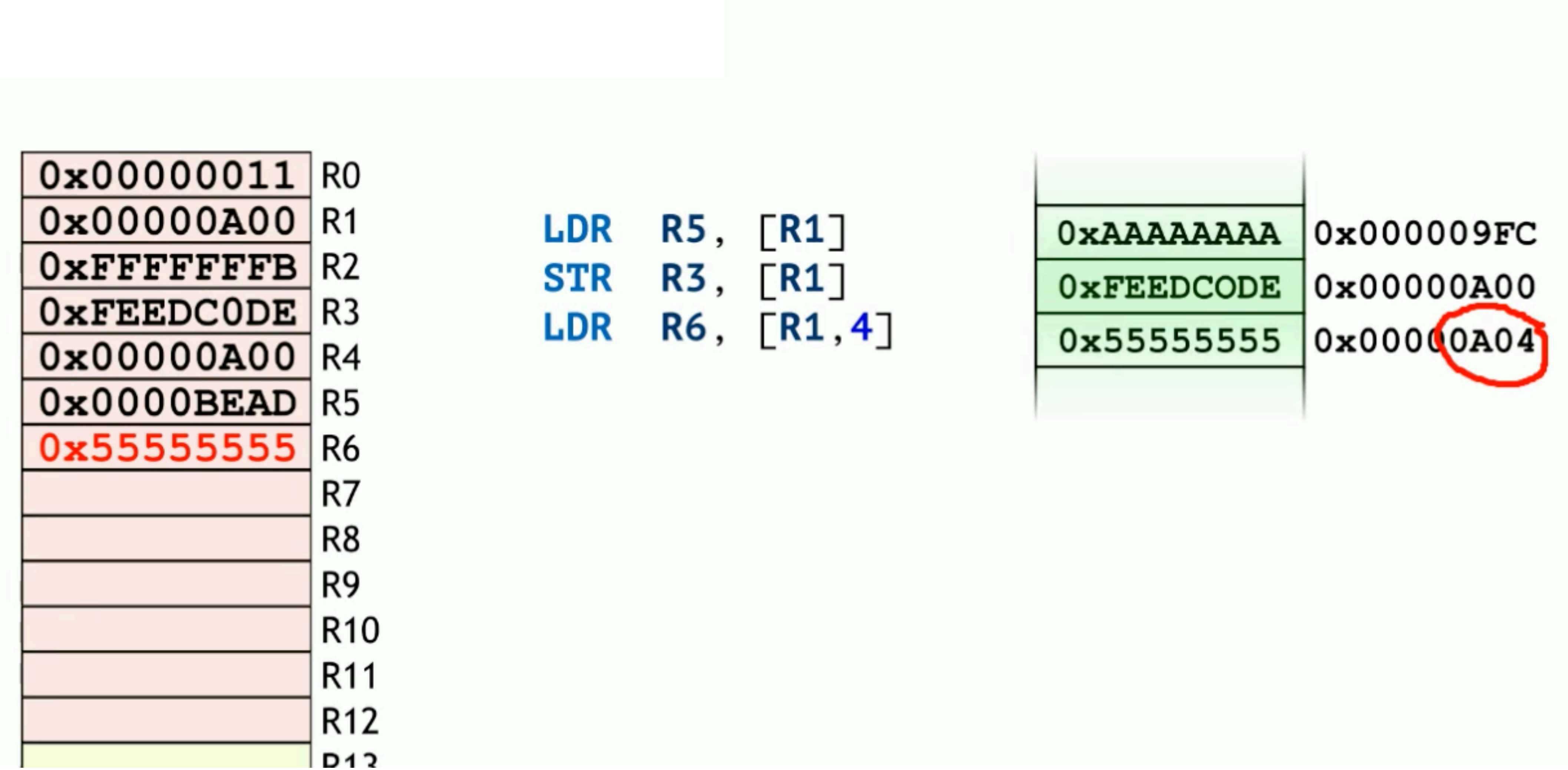

0x00000011	R0
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0x00000A00	R4
0x0000BEAD	R5
0x55555555	R6
	R7
	R8
	R9
	R10
	R11
	R12
	R13

```
LDR   R5, [R1]
STR   R3, [R1]
LDR   R6, [R1,4]
```

0xAAAAAAAA	0x000009FC
0xFEEDC0DE	0x00000A00
0x55555555	0x00000A04

An Example ISA: ARM Cortex 7

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- Arithmetic Operators : addition

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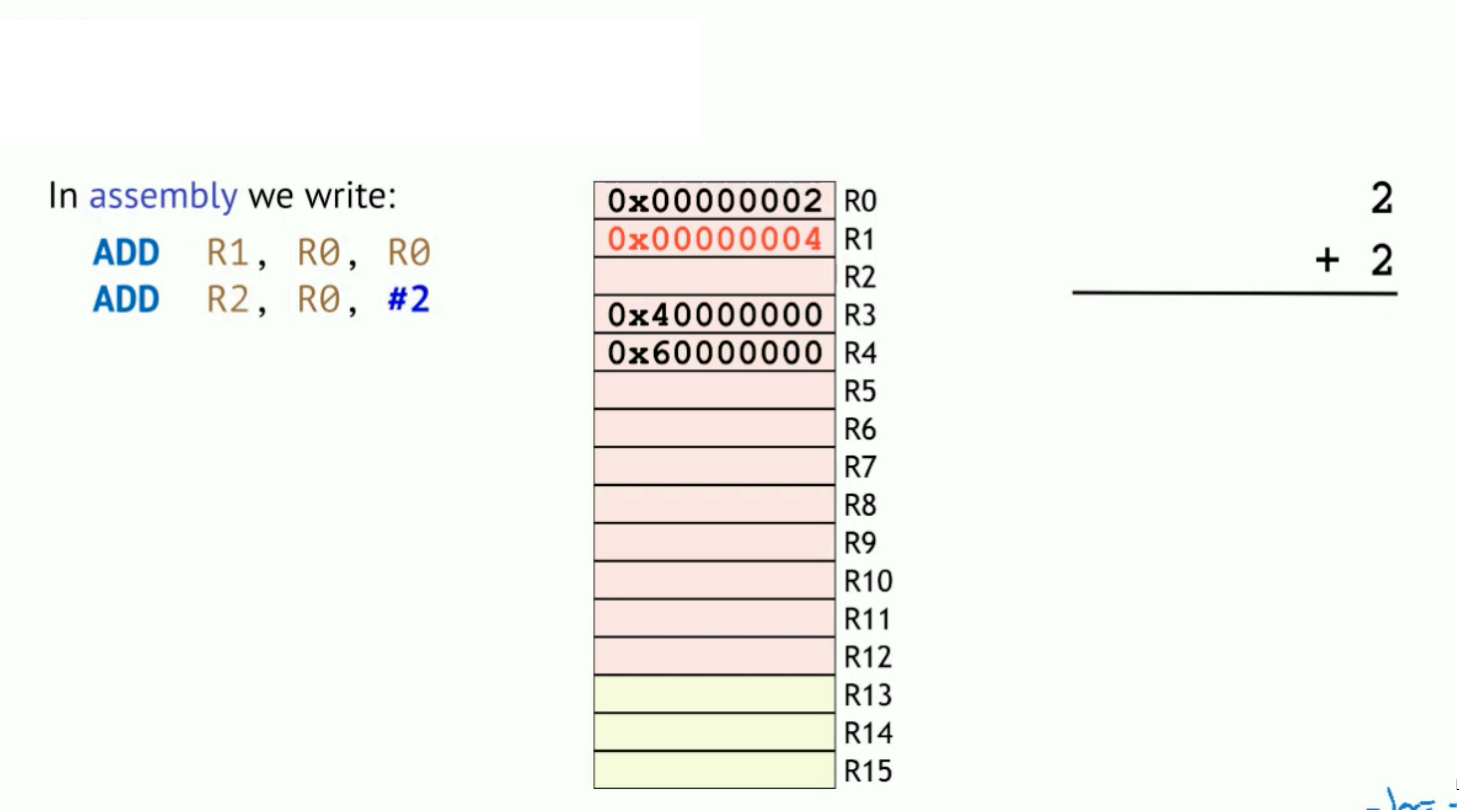

In assembly we write:

```
    ADD   R1, R0, R0
    ADD   R2, R0, #2
```

0x00000002	R0
0x00000004	R1
	R2
0x40000000	R3
0x60000000	R4
	R5
	R6
	R7
	R8
	R9
	R10
	R11
	R12
	R13
	R14
	R15

$$\begin{array}{r} 2 \\ +\ 2 \\ \hline \end{array}$$

An Example ISA: ARM Cortex 7

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- Attention: 2s complement calculations !!!

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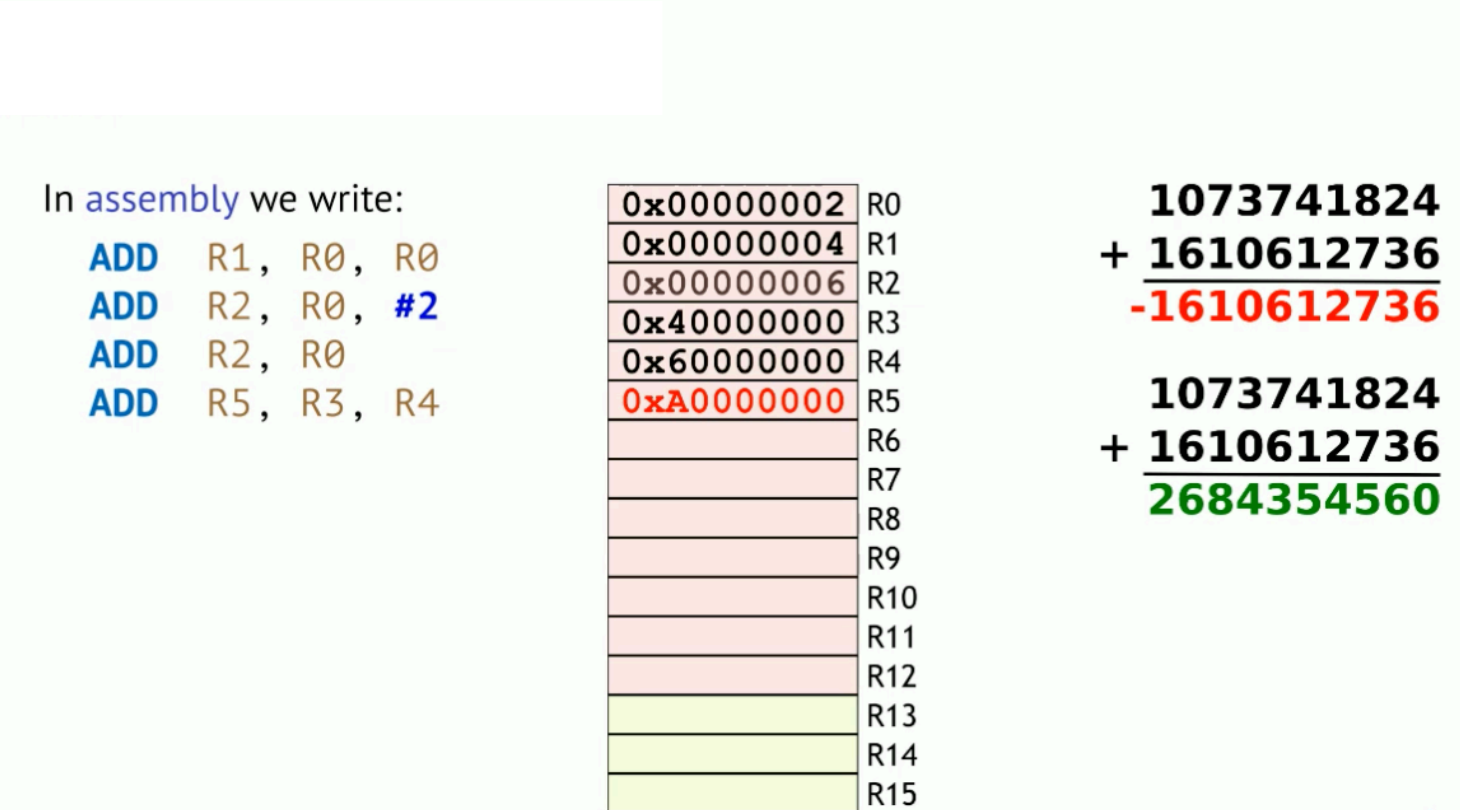


In assembly we write:

```
ADD   R1, R0, R0
ADD   R2, R0, #2
ADD   R2, R0
ADD   R5, R3, R4
```

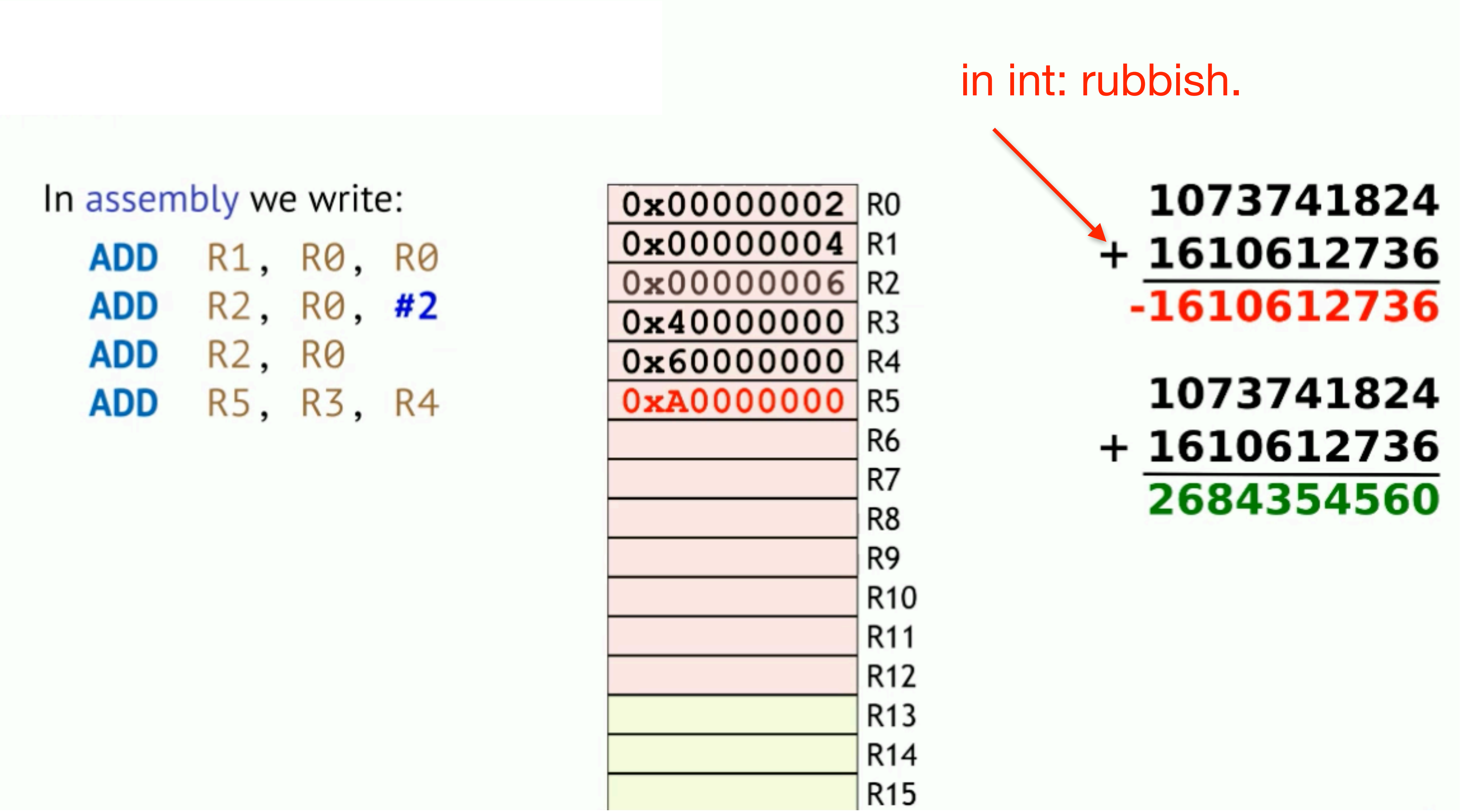
0x00000002	R0
0x00000004	R1
0x00000006	R2
0x40000000	R3
0x60000000	R4
0xA0000000	R5
	R6
	R7
	R8
	R9
	R10
	R11
	R12
	R13
	R14
	R15

```
  1073741824
+ 1610612736
 -1610612736

  1073741824
+ 1610612736
  2684354560
```

An Example ISA: ARM Cortex 7

- Attention: 2s complement calculations !!!



in int: rubbish.

In assembly we write:

```
ADD   R1, R0, R0
ADD   R2, R0, #2
ADD   R2, R0
ADD   R5, R3, R4
```

0x00000002	R0
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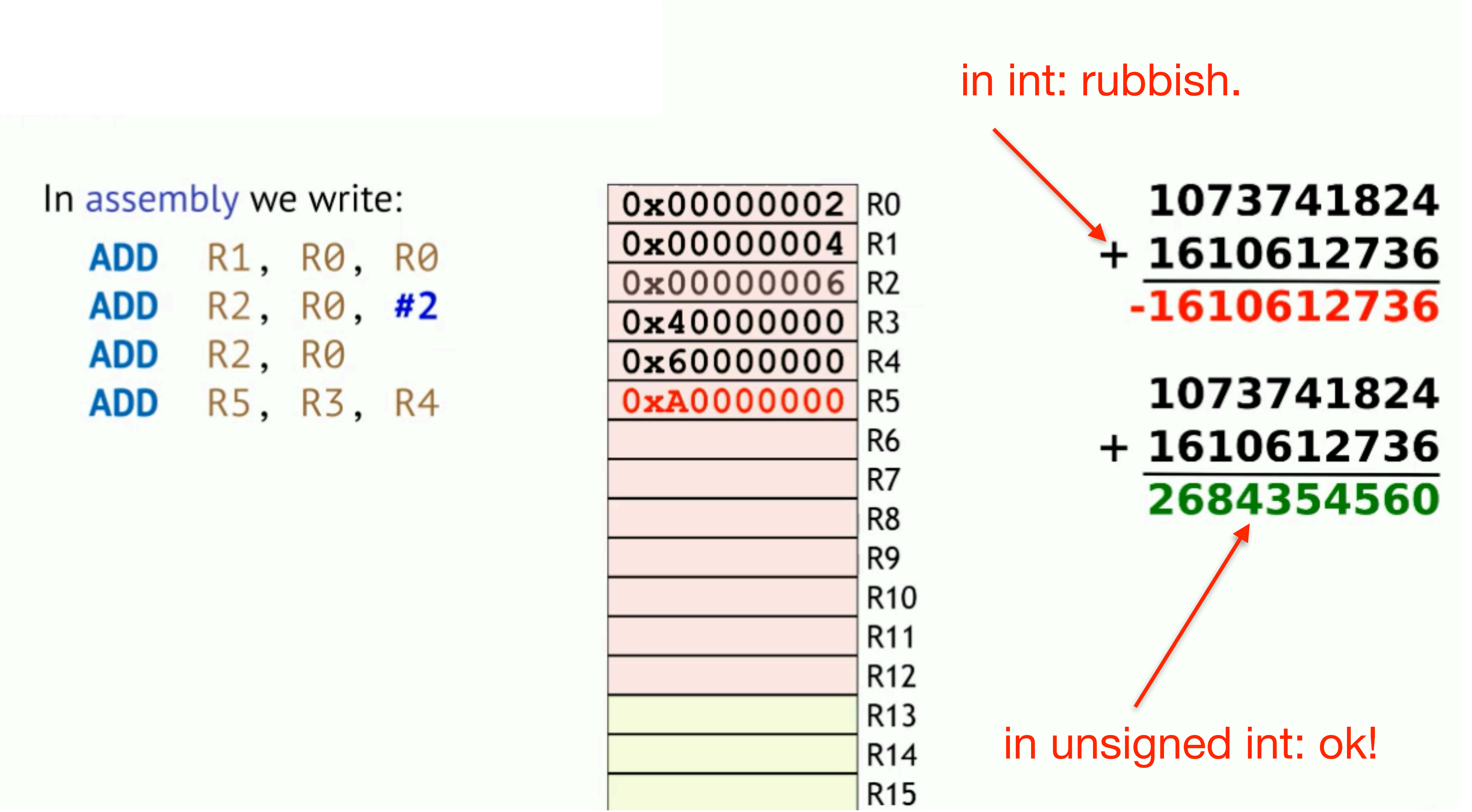
	R6
	R7
	R8
	R9
	R10
	R11
	R12
	R13
	R14
	R15

$$\begin{array}{r} 1073741824 \\ +\ 1610612736 \\ \hline -1610612736 \end{array}$$

$$\begin{array}{r} 1073741824 \\ +\ 1610612736 \\ \hline 2684354560 \end{array}$$

An Example ISA: ARM Cortex 7

- Attention: 2s complement calculations !!!



In assembly we write:

```
ADD   R1, R0, R0
ADD   R2, R0, #2
ADD   R2, R0
ADD   R5, R3, R4
```

0x00000002	R0
0x00000004	R1
0x00000006	R2
0x40000000	R3
0x60000000	R4
0xA0000000	R5
	R6
	R7
	R8
	R9
	R10
	R11
	R12
	R13
	R14
	R15

in int: rubbish.

$$\begin{array}{r} 1073741824 \\ +\ 1610612736 \\ \hline -1610612736 \end{array}$$

$$\begin{array}{r} 1073741824 \\ +\ 1610612736 \\ \hline 2684354560 \end{array}$$

in unsigned int: ok!

An Example ISA: ARM Cortex 7

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- Arithmetic Operators : multiplication

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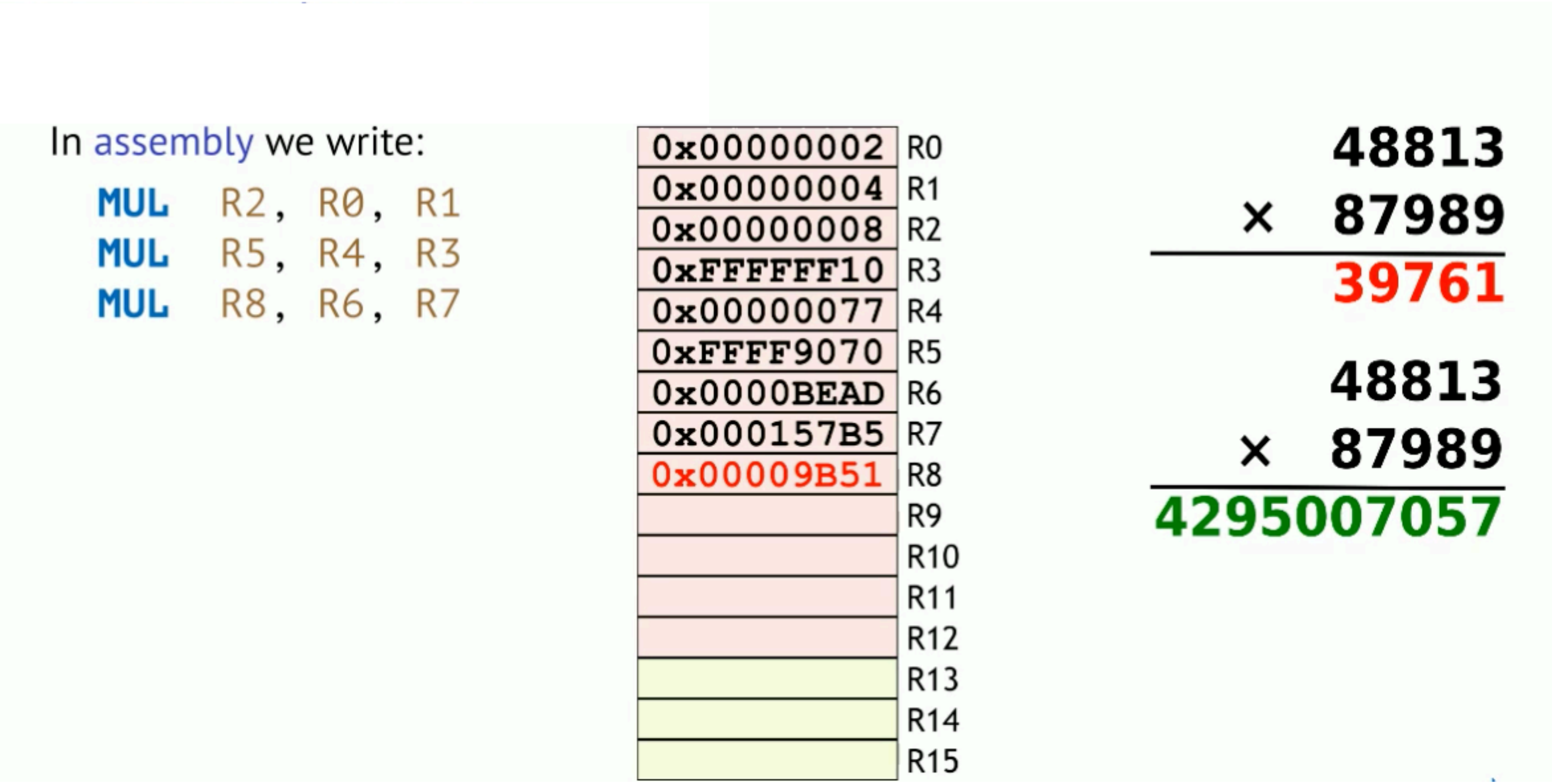

In assembly we write:

```
MUL   R2, R0, R1
MUL   R5, R4, R3
MUL   R8, R6, R7
```

0x00000002	R0
0x00000004	R1
0x00000008	R2
0xFFFFFF10	R3
0x00000077	R4
0xFFFF9070	R5
0x0000BEAD	R6
0x000157B5	R7
0x00009B51	R8
	R9
	R10
	R11
	R12
	R13
	R14
	R15

$$\begin{array}{r} 48813 \\ \times\ \ 87989 \\ \hline 39761 \end{array}$$

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An Example ISA: ARM Cortex 7

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- Arithmetic Operators :
  2 divisions: signed SDIV et unsigned UDIV.

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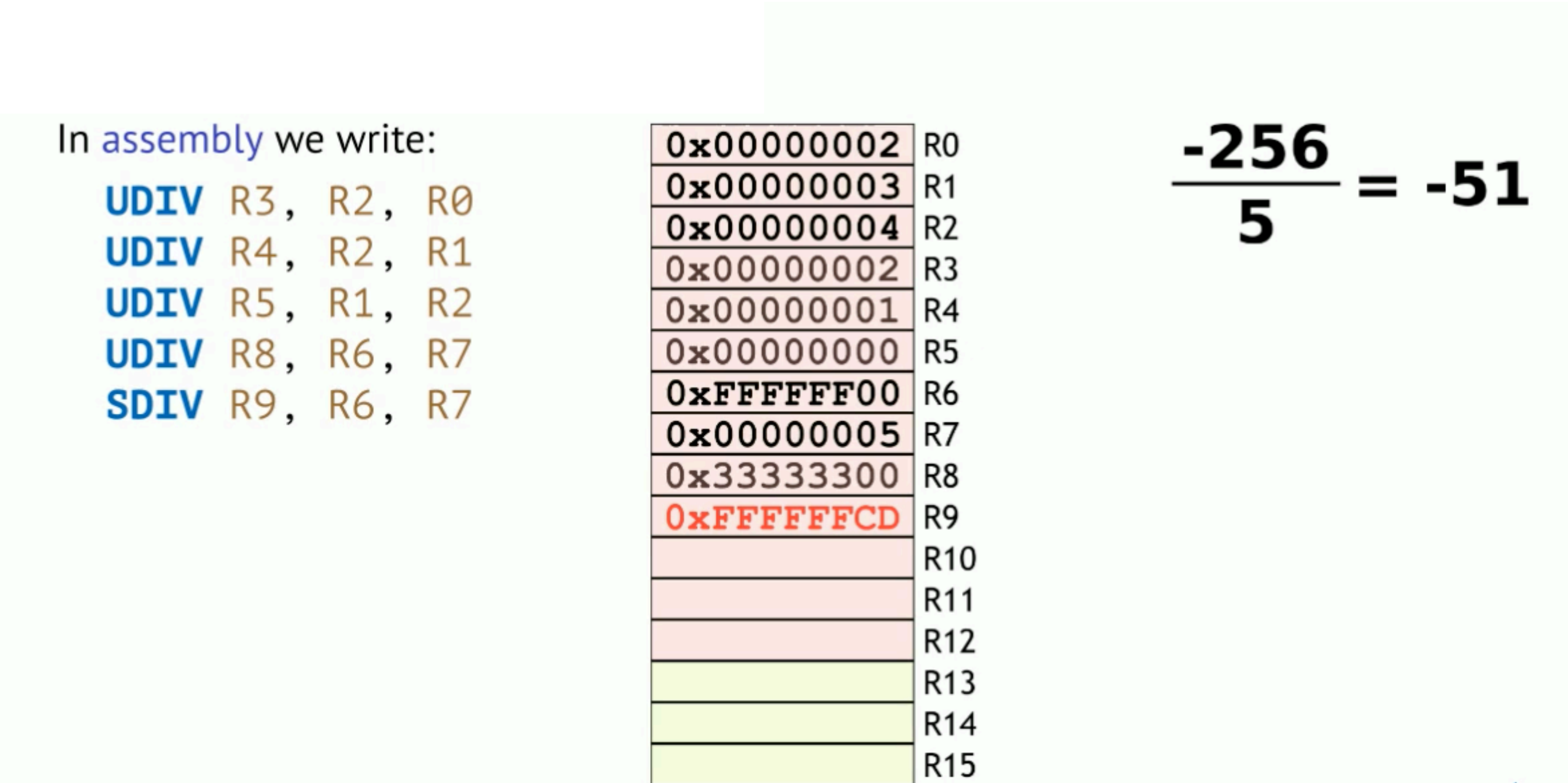

In assembly we write:

```
UDIV R3, R2, R0
UDIV R4, R2, R1
UDIV R5, R1, R2
UDIV R8, R6, R7
SDIV R9, R6, R7
```

0x00000002	R0
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0x00000004	R2
0x00000002	R3
0x00000001	R4
0x00000000	R5
0xFFFFFF00	R6
0x00000005	R7
0x33333300	R8
0xFFFFFFCD	R9
	R10
	R11
	R12
	R13
	R14
	R15

$$\frac{-256}{5} = -51$$

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Does not change APSR !

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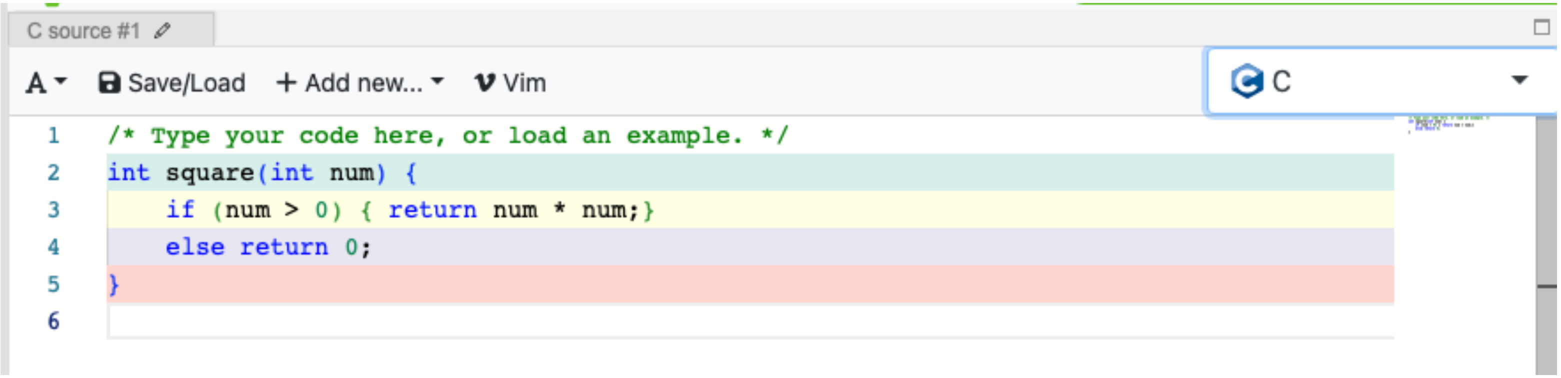

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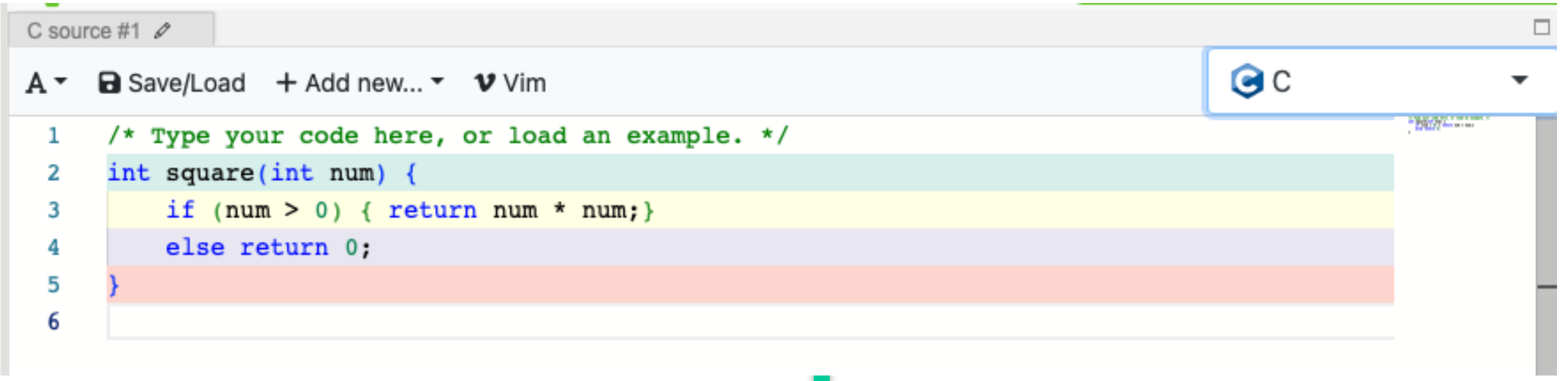

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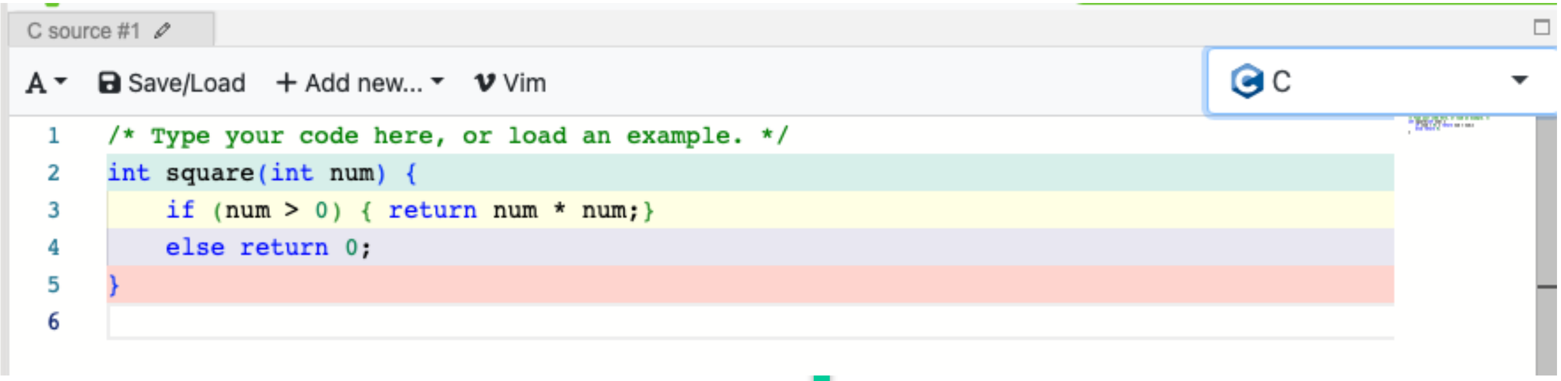

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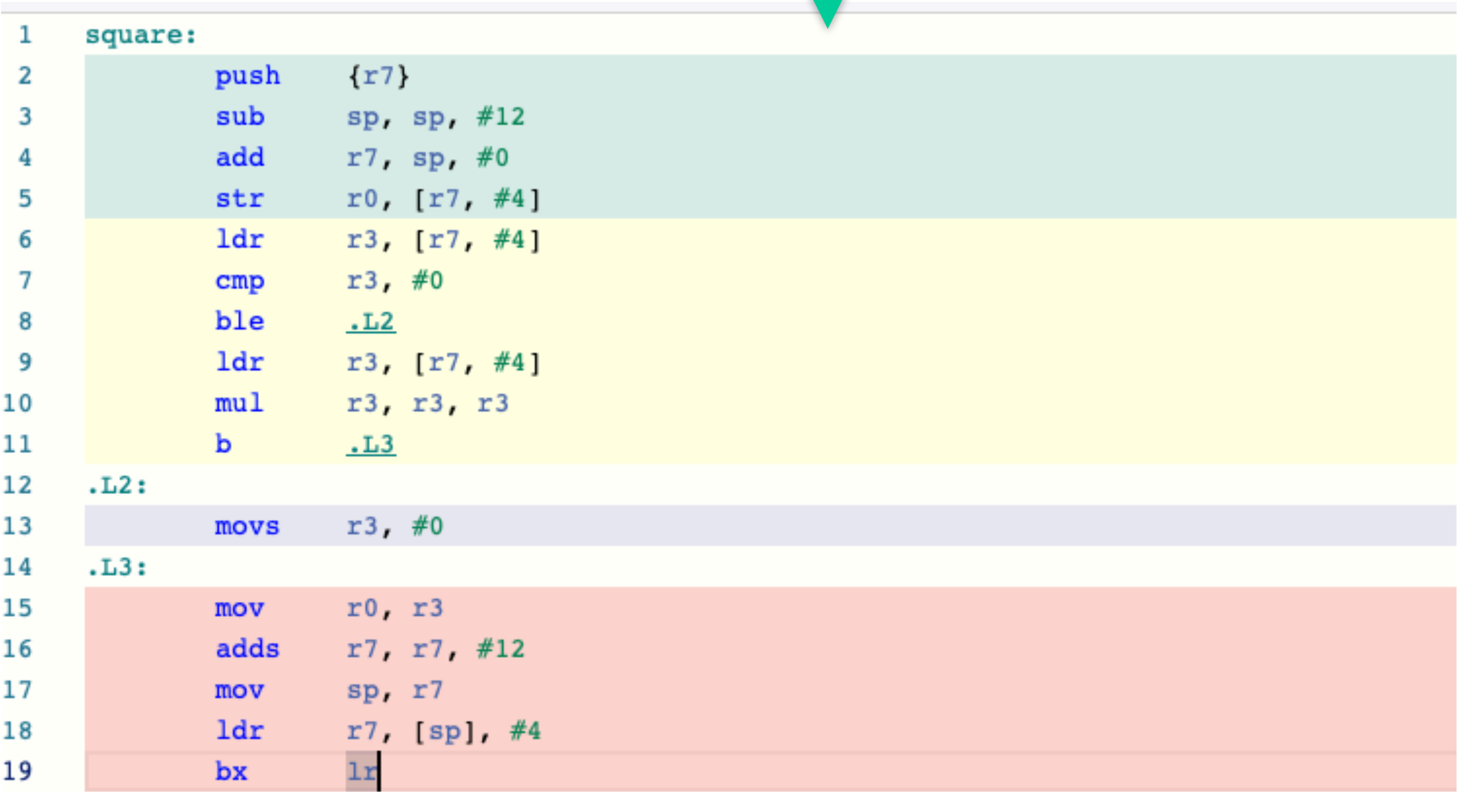

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        ldr     r3, [r7, #4]
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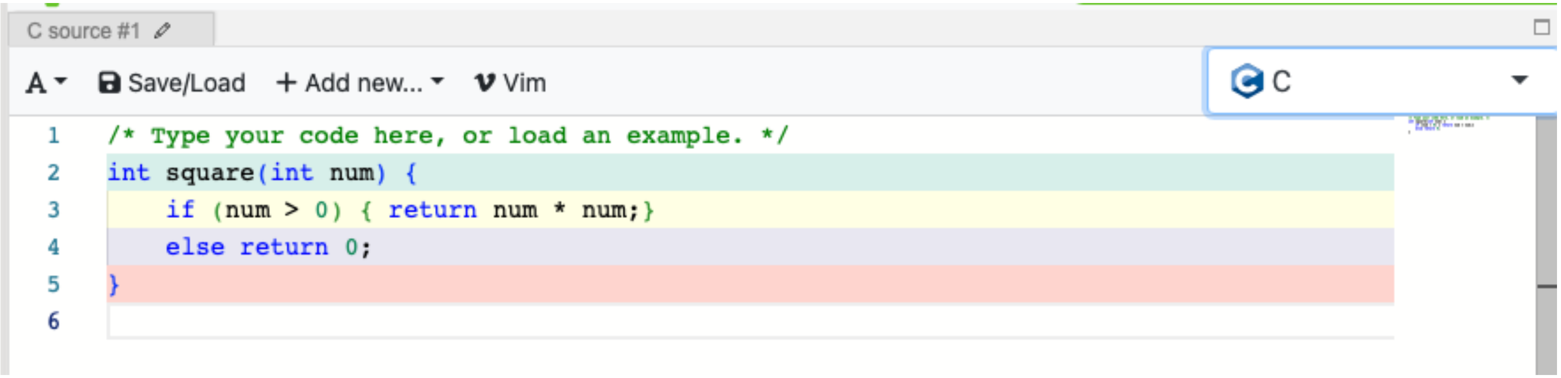

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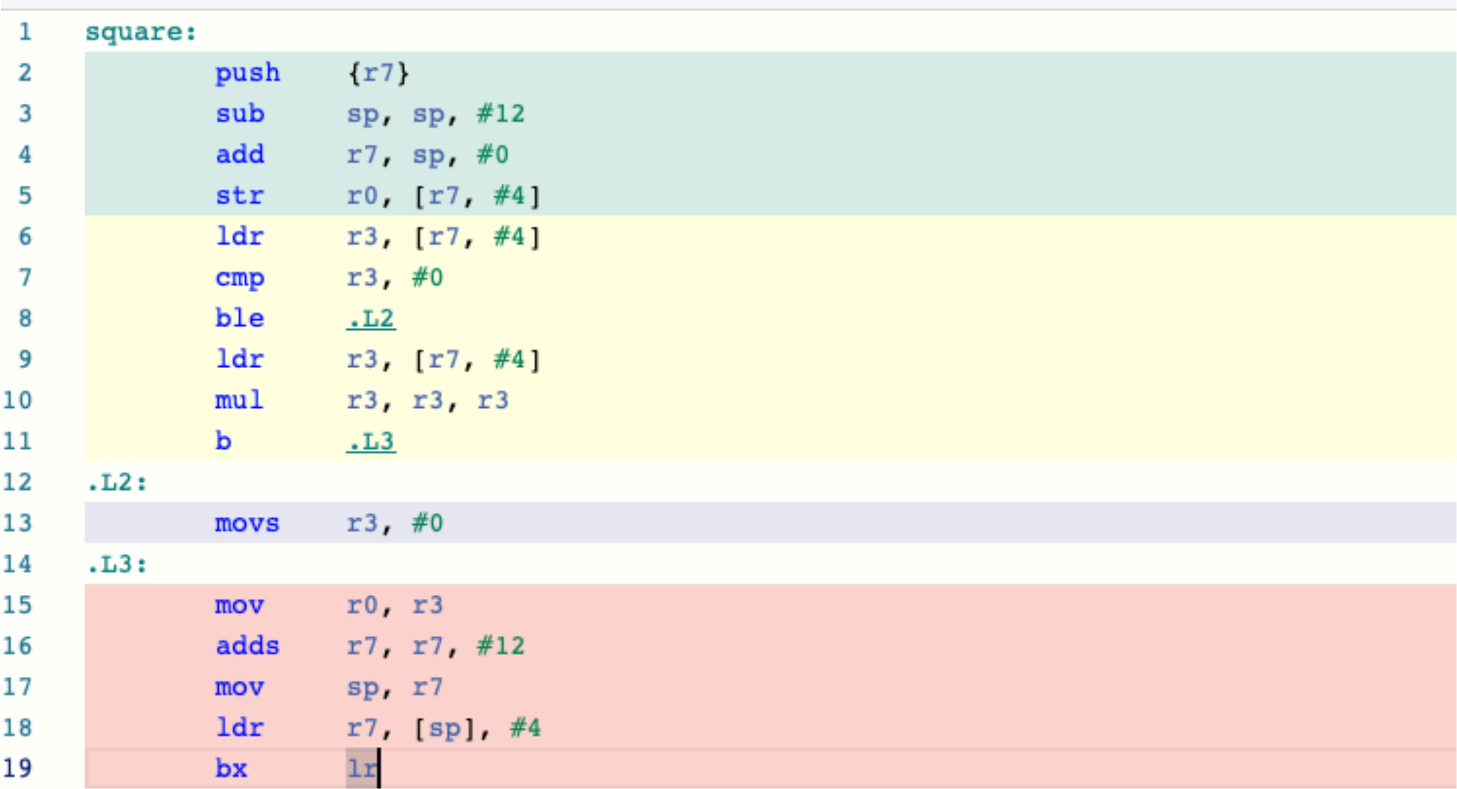

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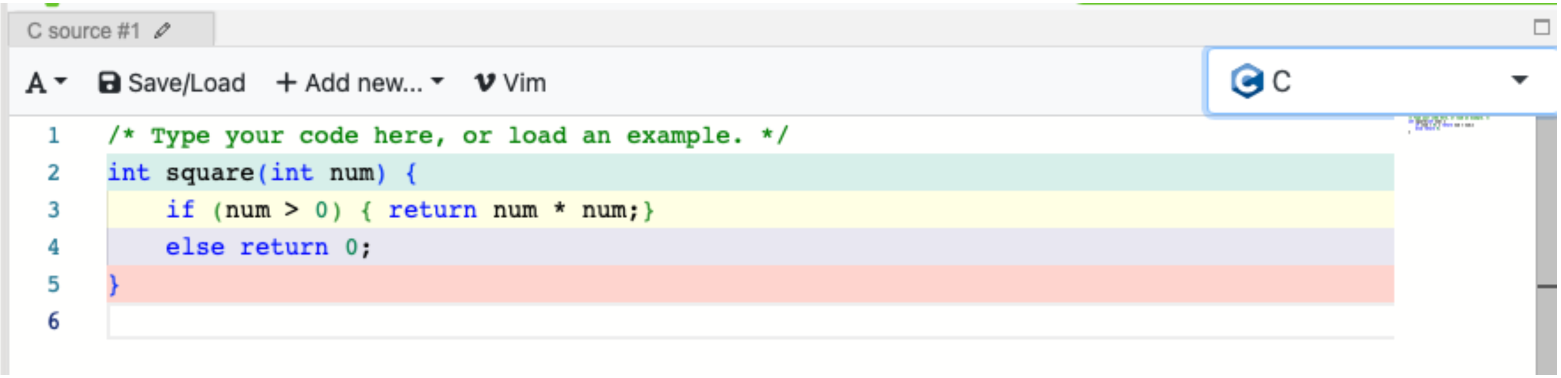

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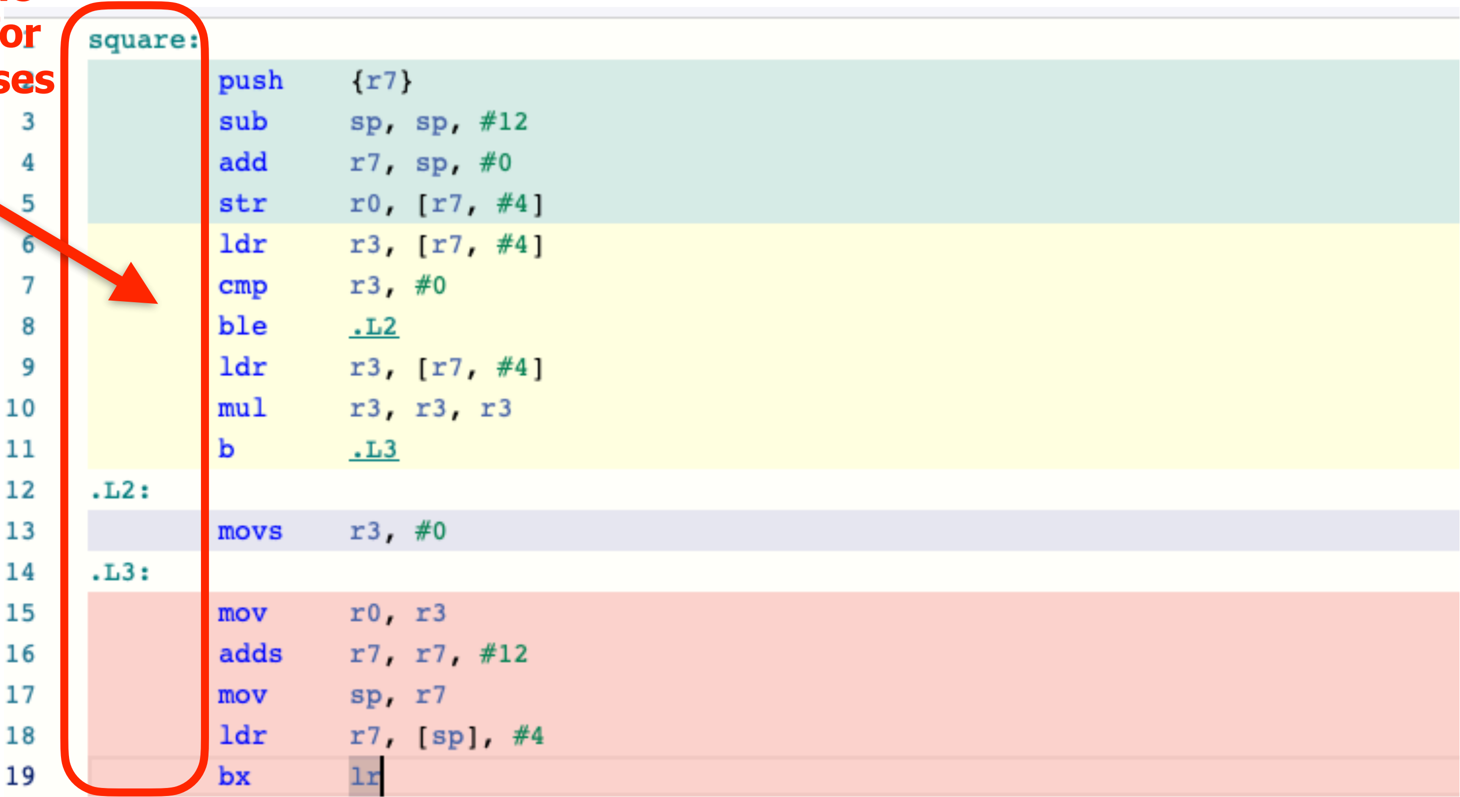
symbolic labels for addresses



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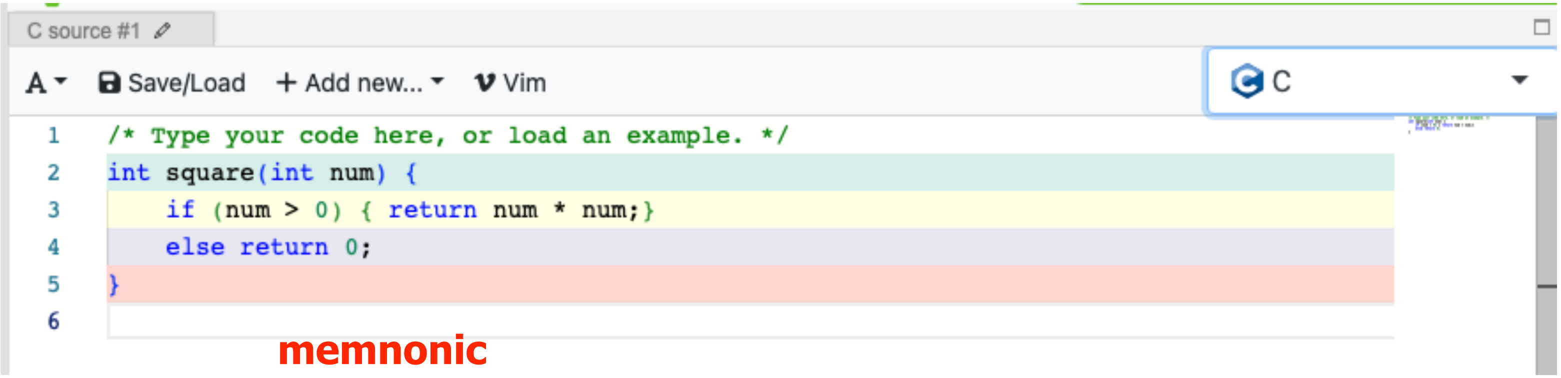

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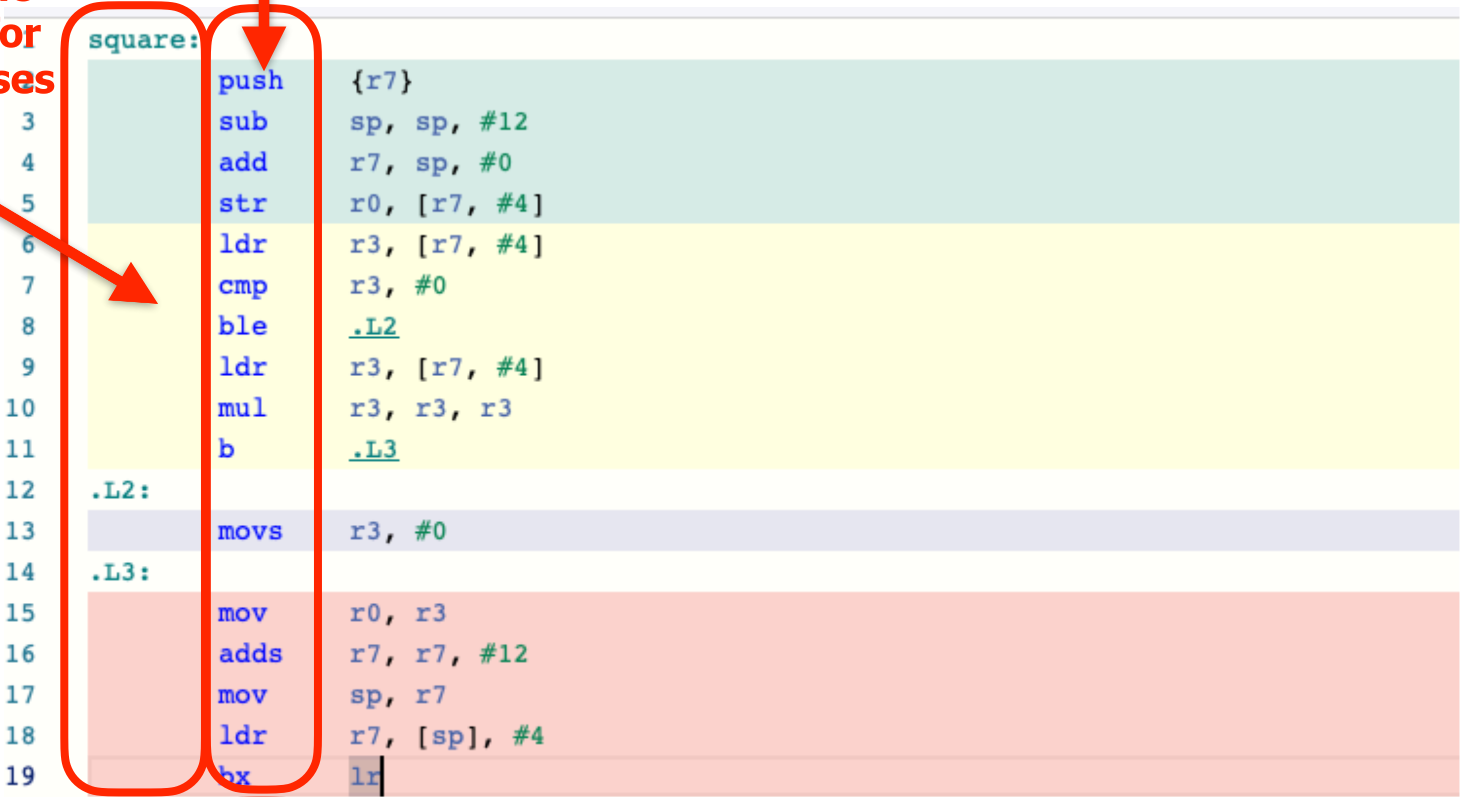

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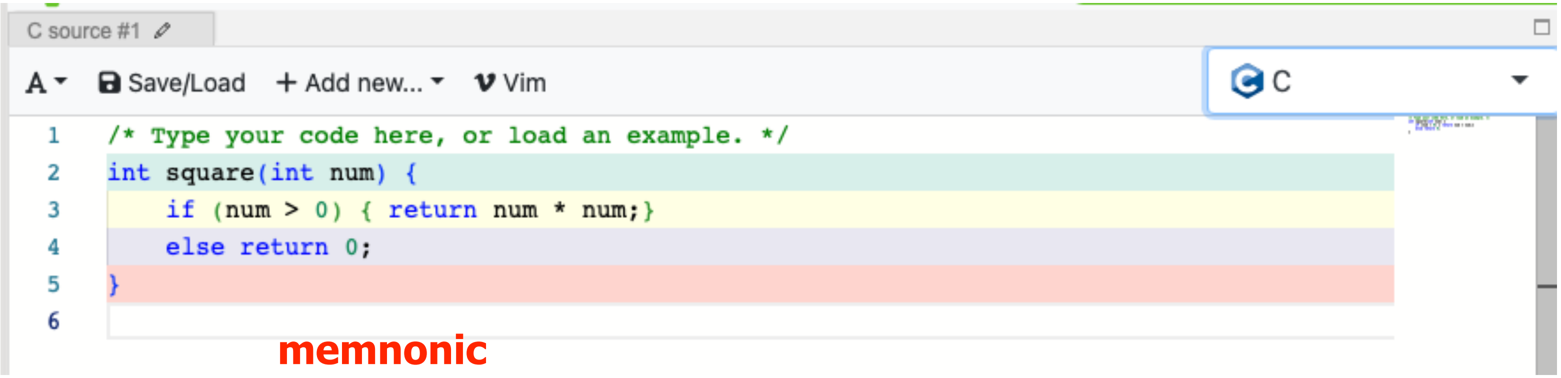

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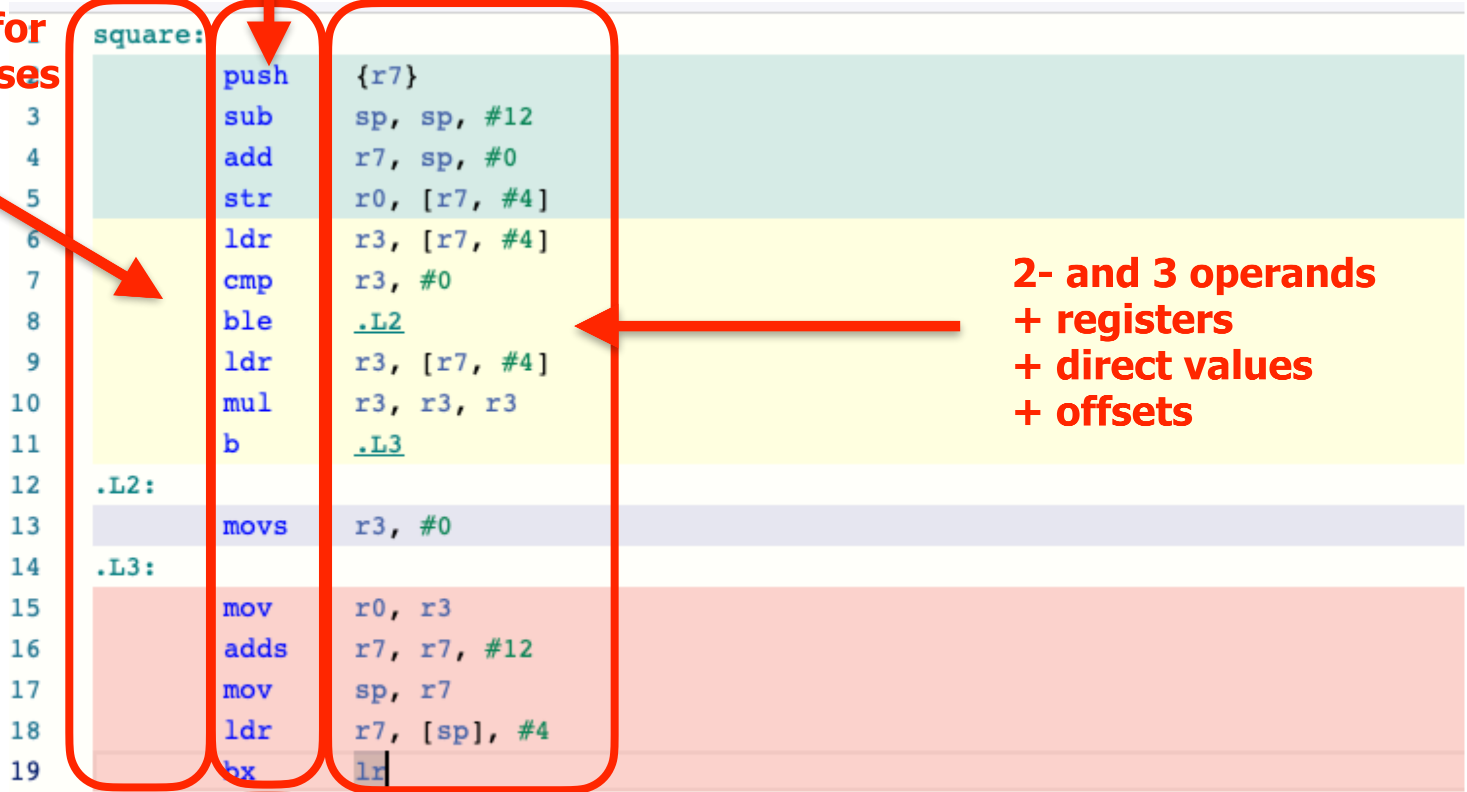

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2- and 3 operands
+ registers
+ direct values
+ offsets

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```
datatype reg = r0 | r1 | r2 | r3 | r4 | r5 | r6 | r7 | sp | lr | pc

datatype opcode = MOV | MVN | MOVW | MOVT | LDR | STR
                | ADD | SUB | MUL | UDIV | SDIV
                | B | BX | BLE | BEQ | BNQ | CBX | CMP

datatype varg = none                         (“---")
              | direct nat                   ("# _")
              | register2 reg reg            ("_,_")
              | register_indirect reg        ("[_]")
              | register_indirect_offset reg nat ("[_,_]")

datatype com = label nat ("⟨L _⟩”)
             | branch opcode nat ("⟨_ L _⟩")
             | instruction opcode reg varg ("⟨_,_,_⟩")
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- SAMPLE: [⟨MOV,r3,#5⟩,⟨ADD,r5,r3,r4⟩,⟨L 2⟩,⟨ADD,r5,r3,r4⟩,⟨BLE,r5,[r3,4]⟩]

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  - inherited and synthesised attributes

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$$
\begin{aligned}
&Lab_{out}(e) = Lab_{in}(b) \wedge \\
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&Env_{in}(a) = Env_{in}(e) \wedge \\
&Env_{in}(b) = Env_{in}(e) \wedge \\
&Code_{out}(e) = Code_{out}(a) \\
&\qquad @ [\langle CMP,r7,\#0\rangle] \\
&\qquad @ [\langle BEQ\ L\ Lab_{in}(e)+1\rangle] \\
&\qquad @\ Code_{out}(b) \\
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@ [⟨CMP,r7,#0⟩]

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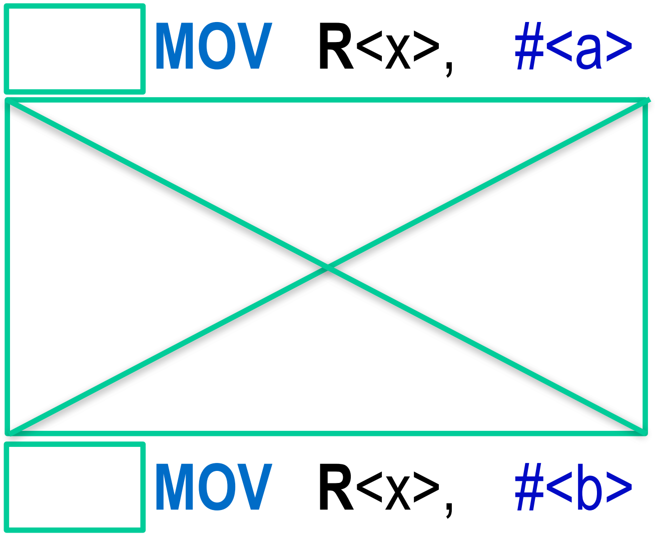

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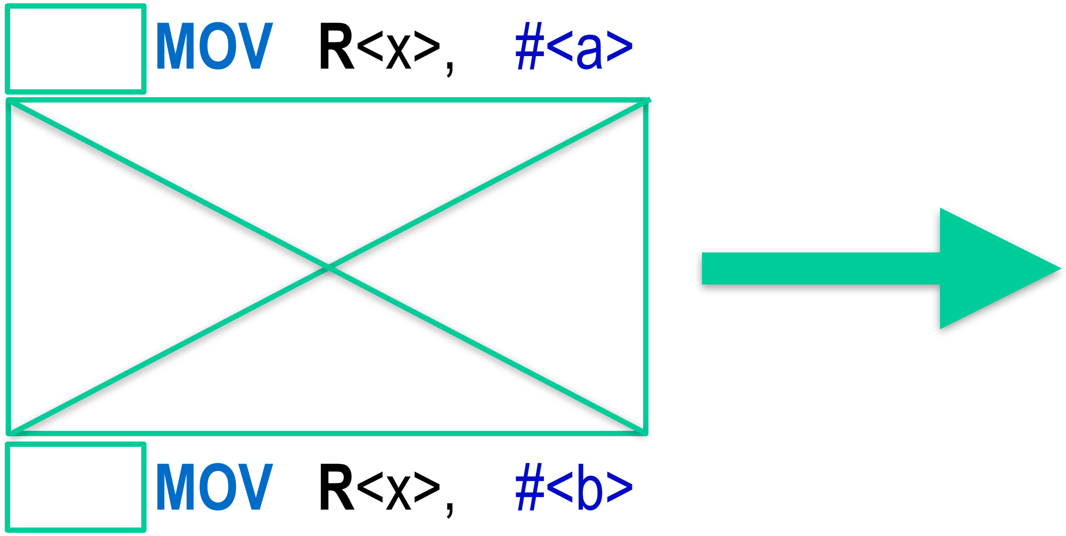

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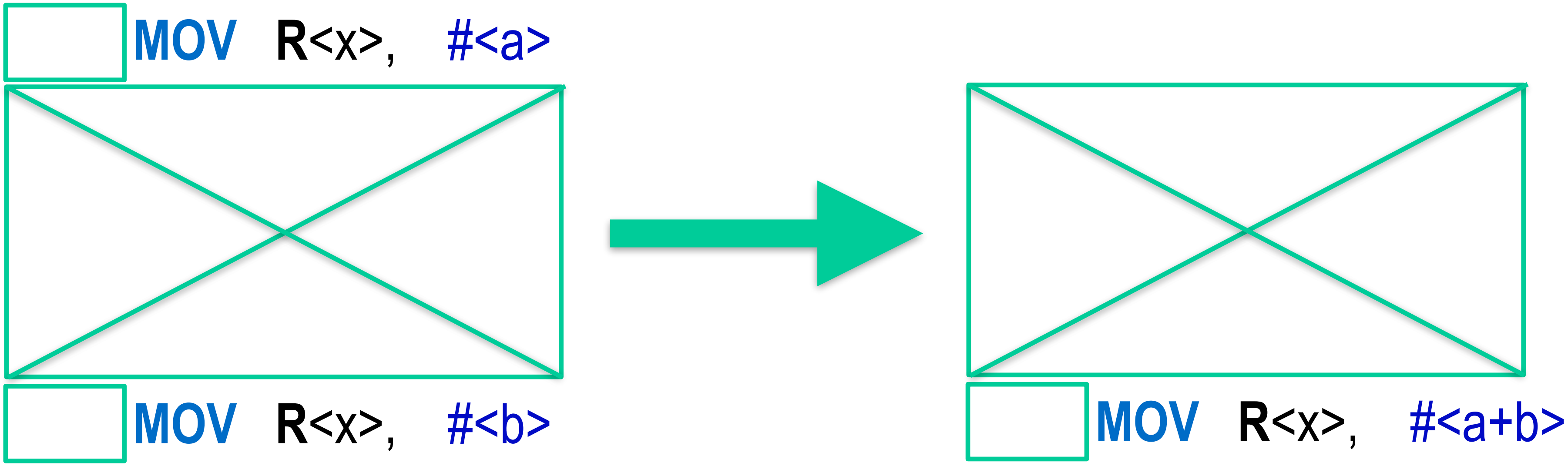

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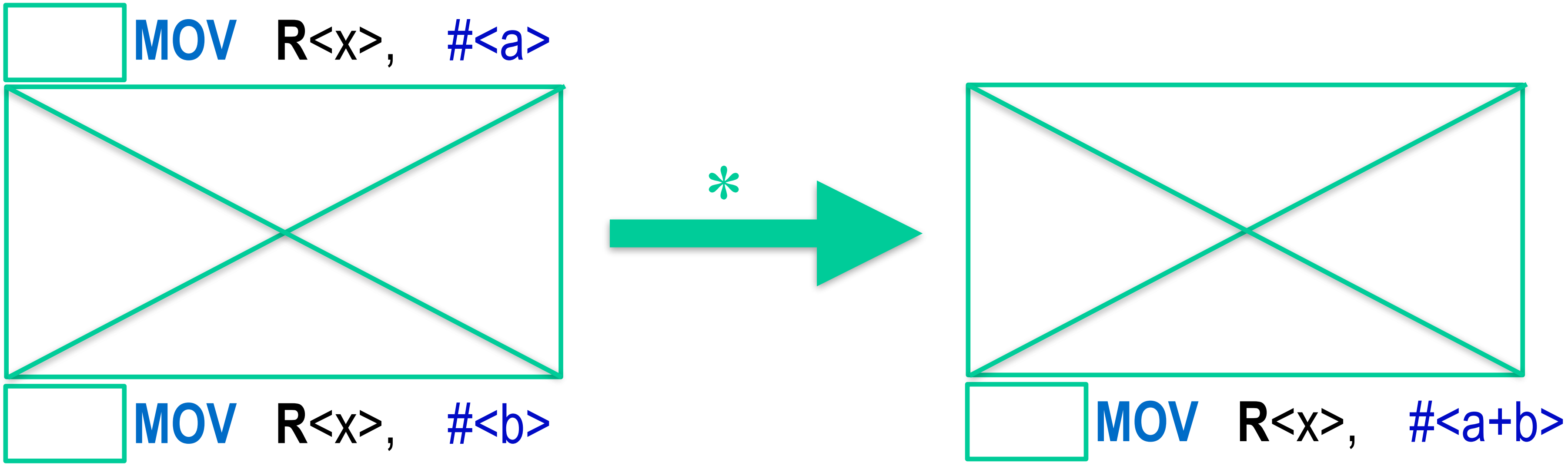

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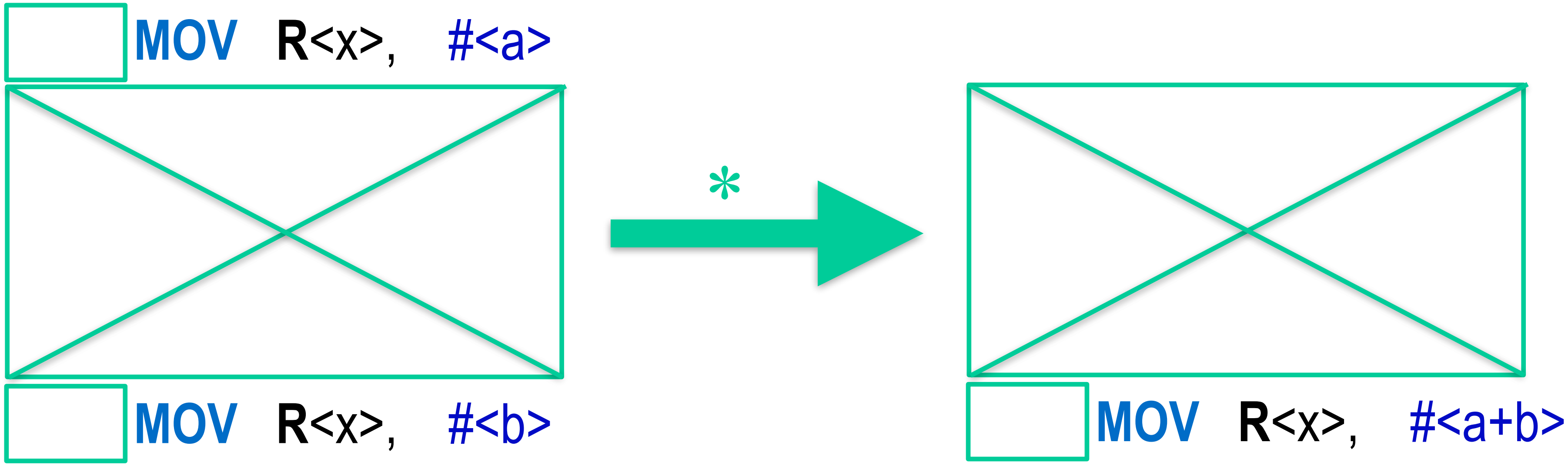

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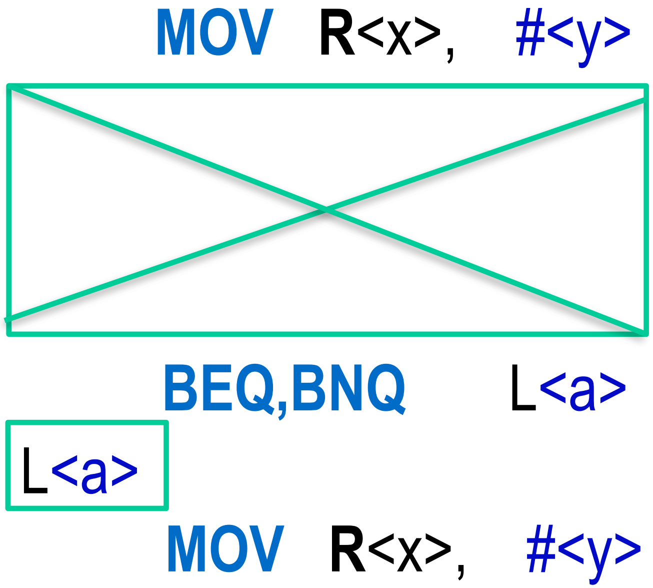

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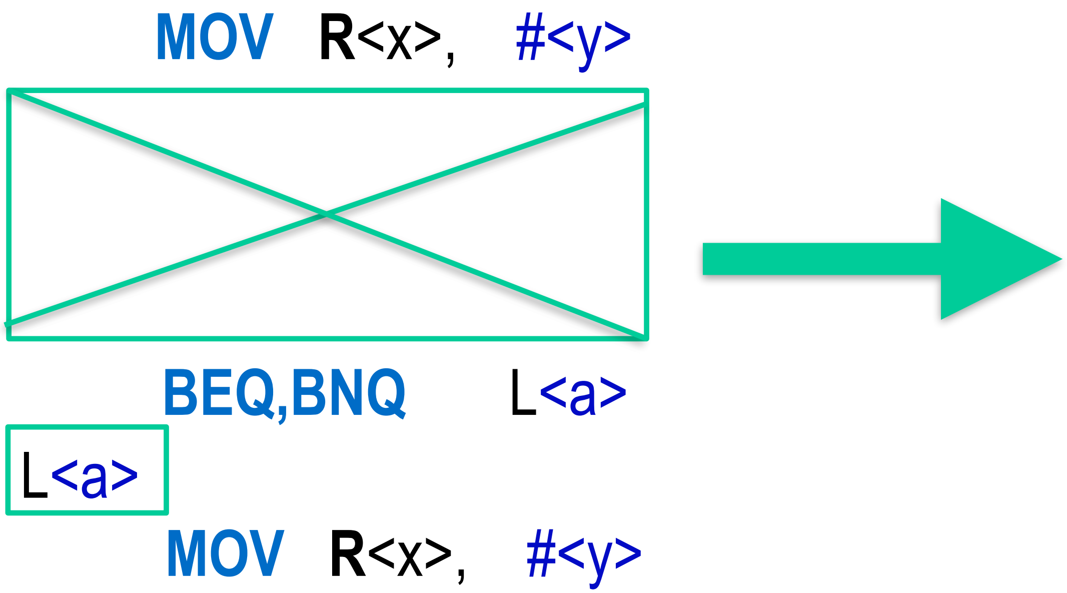

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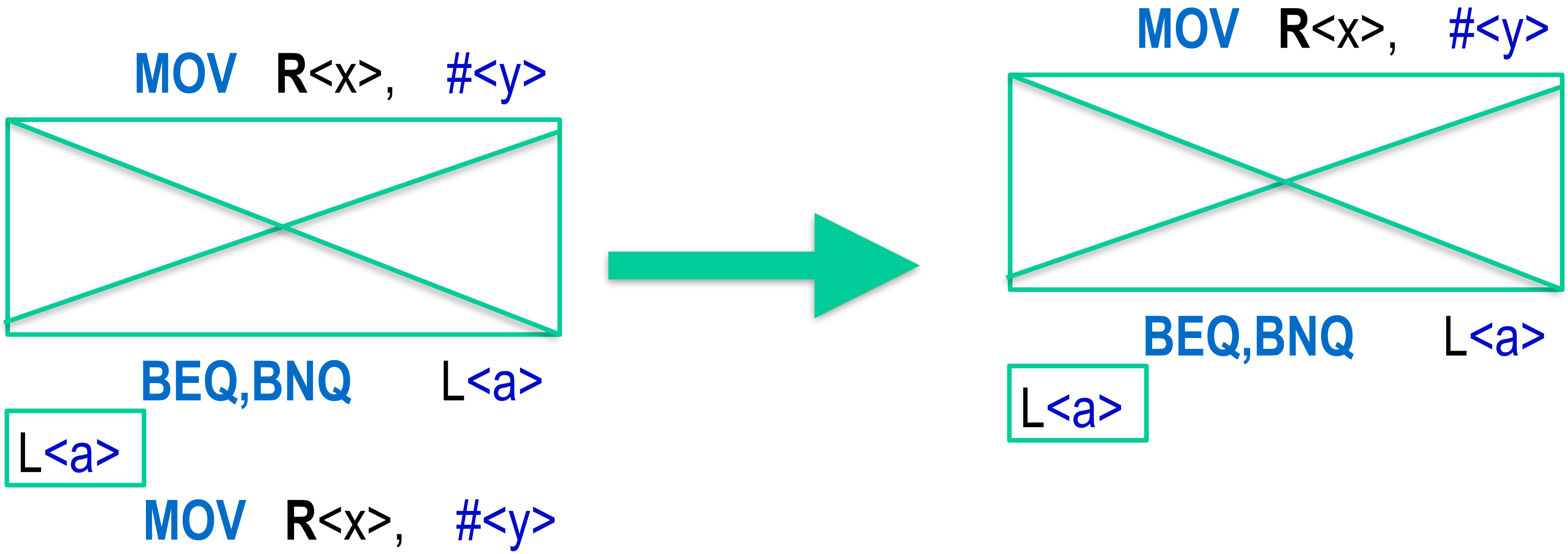

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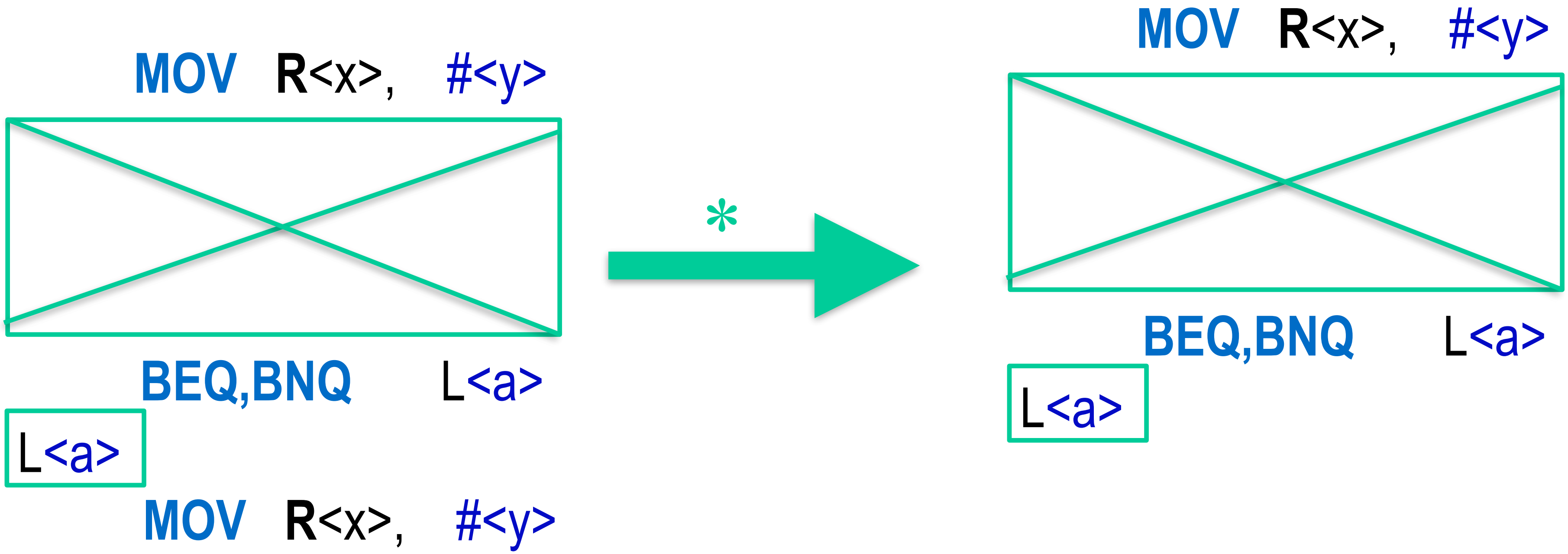

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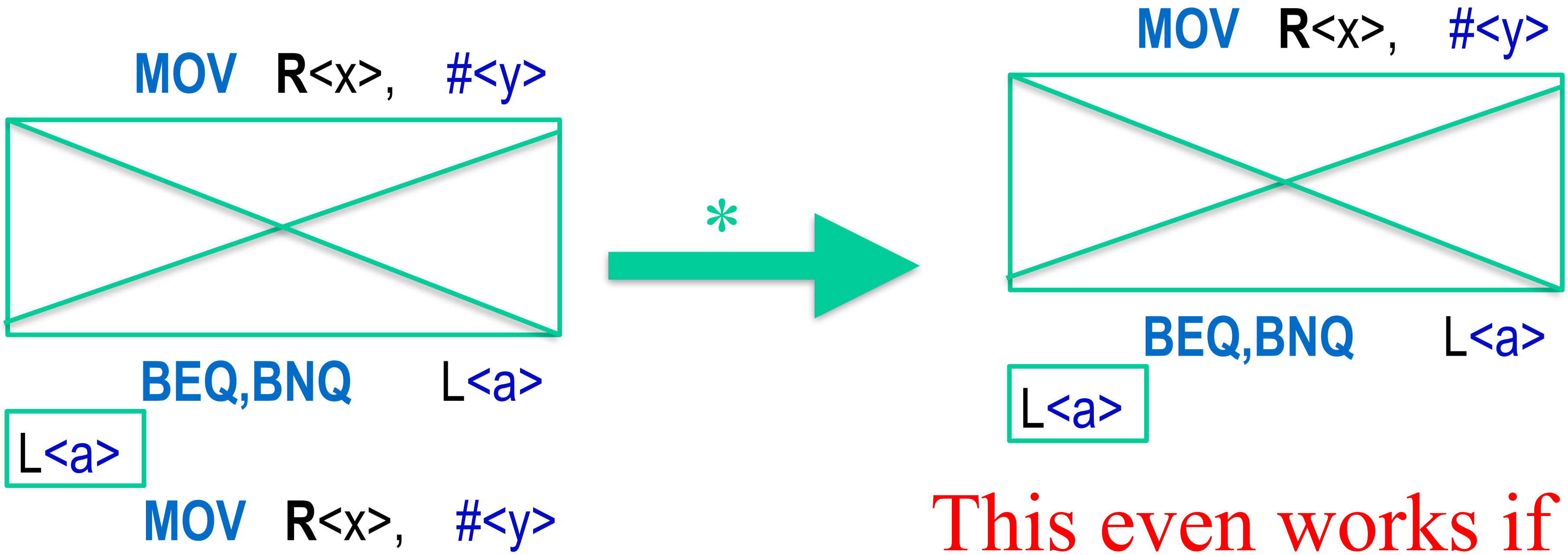

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This even works if the types are different in the source language !

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MUL  R<x>, R<y>, #0x2          ADD  R<x>, R<y>, R<y>
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In some architectures, this is mapped to SHL (shift-left)

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References

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